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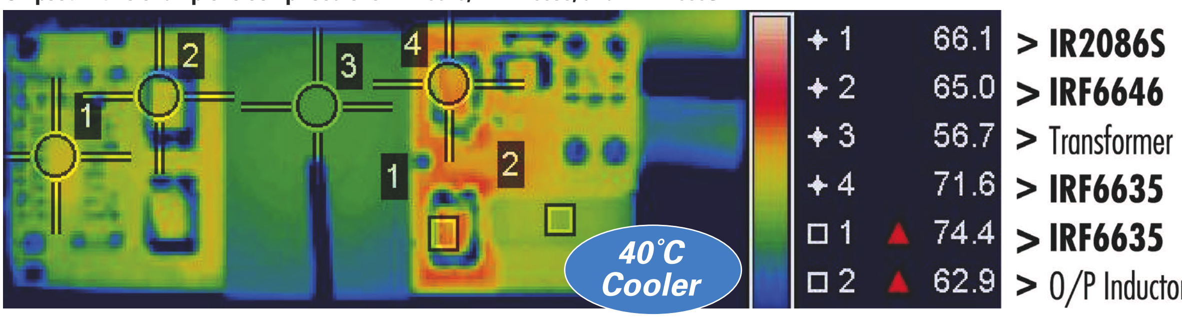

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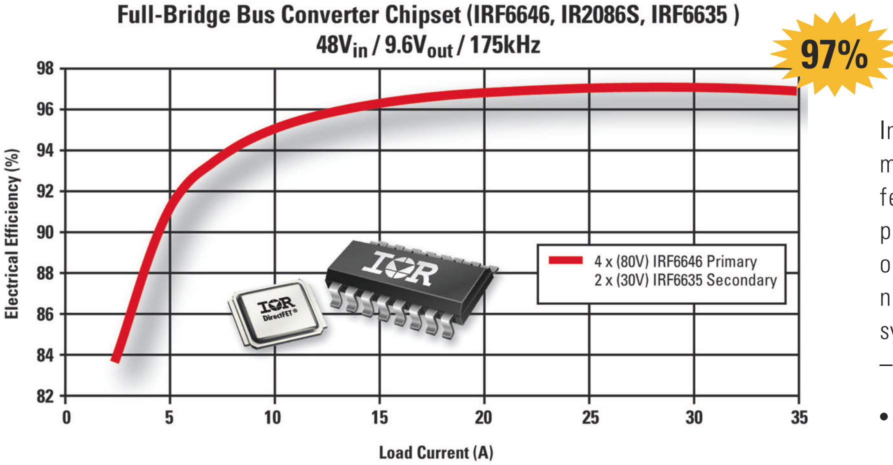

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IRF6646	Medium can	80V	9.5mΩ	36nC	12nC
IRF6638	Medium can	30V	2.9mΩ	30nC	11nC
IRF6635	Medium can	30V	1.8mΩ	47nC	17nC
IRF6631	Small can	30V	7.8mΩ	12nC	4.4nC
IRF6629	Medium can	25V	2.1mΩ	34nC	11nC
IRF6628	Medium can	25V	2.5mΩ	31nC	12nC
IRF6622	Small can	25V	6.3mΩ	11nC	3.8nC

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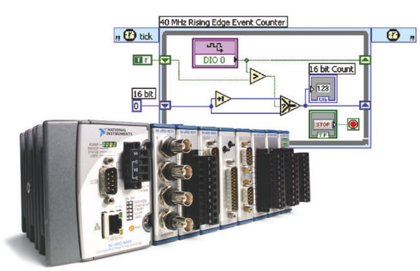

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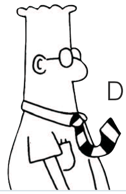

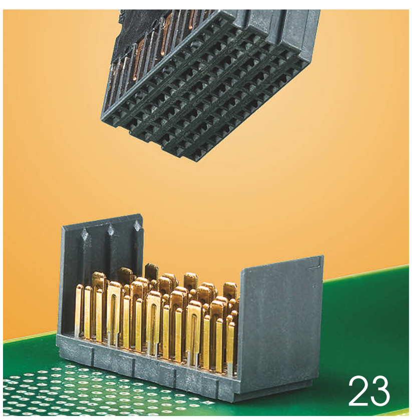

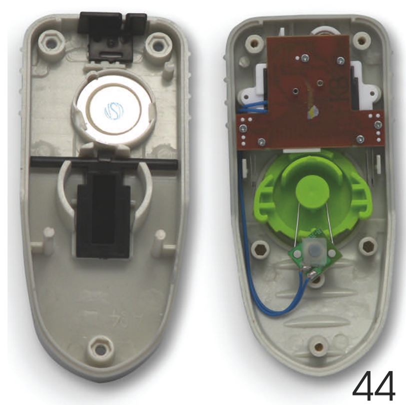

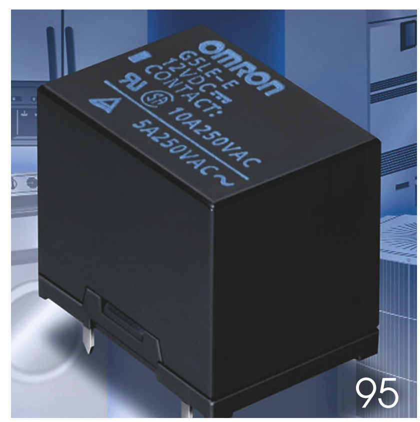

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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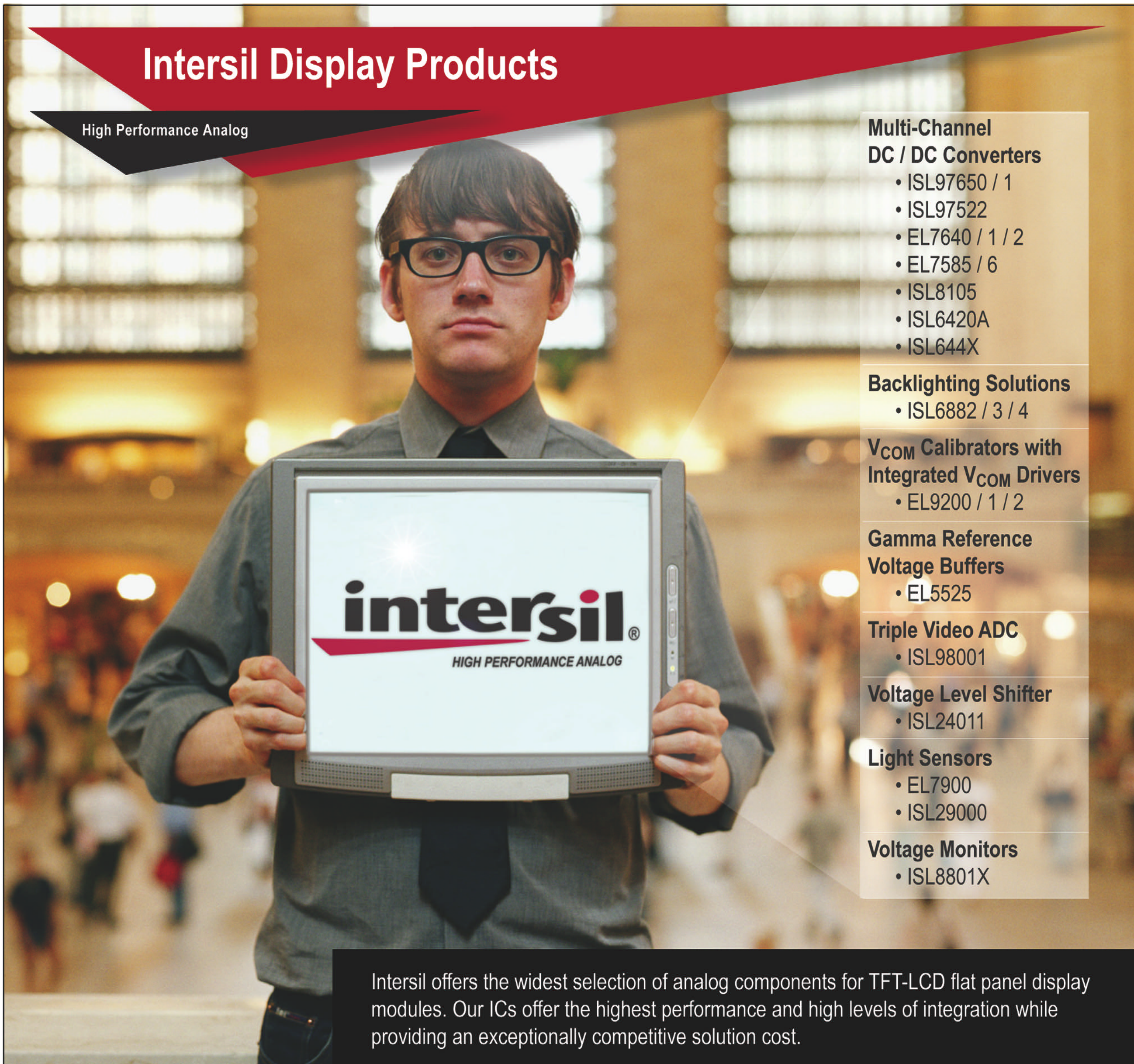

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BY PAUL RAKO, TECHNICAL EDITOR

DRM cripples digital video from PCs to TVs

As I researched 45-in. LCD panels for an upcoming article, it became clear that insidious forces are trying to prevent users from employing any new TV as a PC monitor. There are no new 45- to 47-in. LCD panels that can accept a digital signal from an older computer. The digital HDMI (high-definition-multimedia-interface) inputs on TVs have HDCP (high-bandwidth digital-content protection). This situation is a DRM (digital-rights-management) system that media companies and the government forced on the manufacturers. You can buy a new video card that has HDCP, but DRM locks out home-built systems, and only big companies will be able to produce a PC that can render 1080p signals on a TV (**Reference 1**). If, like me, you have an AGP (Advanced Graphics Processor)-bus computer, you would also need to buy a new computer, because the new HDCP cards are available with a PCIe (Peripheral Component Interconnect Express) bus.

I own a Sharp LC-45GD7U LCD TV that allows me to display 1080p signals through the HDCP port. Allowing 1080p digital input from a computer was an oversight that almost every manufacturer soon remedied. Some LCD panels, such as the Vizio (www.vizio.com) GV47LF spec only 1360×768 pixels through the analog D-sub connector and only 480×640 pixels through the digital HDMI port. (Yet some forum users claim that the Vizio synchronizes with 1920×1080 pixels through the analog port.) Equally frustrating is the confusion over progressive scan. Some LCD-panel models, such as the Samsung (www.samsung.com) LN-S4695 and LN-S4696 and the Toshiba (www.toshiba.com) 47LX196 and 47LZ196, seem identical. The manufacturers' Web sites disclose no differences other than a couple of connectors and a few hundred dollars.

However, forum and newsgroup users explain that higher digit model numbers accept progressive-scan 1080 signals. But where do the TVs accept these signals? Both models of the Samsung accept 1080p through the analog connector. That fact does not mean that it accepts 1080p from the HDMI; I can guarantee you that the manufacturers have implemented HDCP so that you cannot run the panel from your PC unless you use the analog port.

Some large LCD panels, which lack TV tuners, can display digital signals. The Westinghouse (www.westinghouse.com) LVM-47w1 manual makes clear that it can accept 1080p signals on its two DVI connectors as well as through the analog D-sub connector. I suspect that the Polaroid (www.polaroid.com) FLM-4701 and ByD:sign (www.bydsign.com) d:4742M monitors also accept digital 1080p signals. By hooking up external tuners and set-top boxes, you end up with a TV, but you would have to deal with quite a few remote controls.

If you are considering hooking a PC to a large TV, you may have to resign yourself to using the analog D- sub connector. Carefully do your research before making a purchase. If you see a VGA input, do not assume it is high-definition; the Vizio isn't. If you see a DVI (digital-video-interface) input, do not assume it is high-definition; the Sharp (www.sharpusa.com) isn't. The Mitsubishi (www.mitsubishi.com) LT-46231 DVI input starts looking for HDCP at resolutions higher than 1280×720 pixels. If you see 1080p, don't assume you can get that into the set through the HDMI connector; it might just be a 1080p component in for Blu-ray players and game consoles. Some sets advertise 1080p because the LCD panel is progressive internally, but you cannot get a 1080p signal into the TV from any connector. You may need to do what my buddy Dave did when he bought a Samsung LTP468W: Drag a computer into a high-end-TV showroom and see whether the TV starts up with 1920×1080-pixel resolution.

Toshiba could not tell me whether the analog input of the 47LX196 could render 1920×1080-pixel signals. The lack of clear information on these new TVs is a disgrace to the marketing departments at all the manufacturers. The limitations on your use of these TVs as computer monitors are disgraceful to the engineering departments. For a hardware company to make a product with a 1080p panel and no 1080p PC digital input, well, as Frank Zappa used to say: "If there is a hell, it waits for them."EDN

REFERENCE

1 Doctorow, Cory, "Only big companies' PCs will play high-def DVDs," BoingBoing.net, www.boingboing.net/2006/02/12/only_big_companies_p.html.

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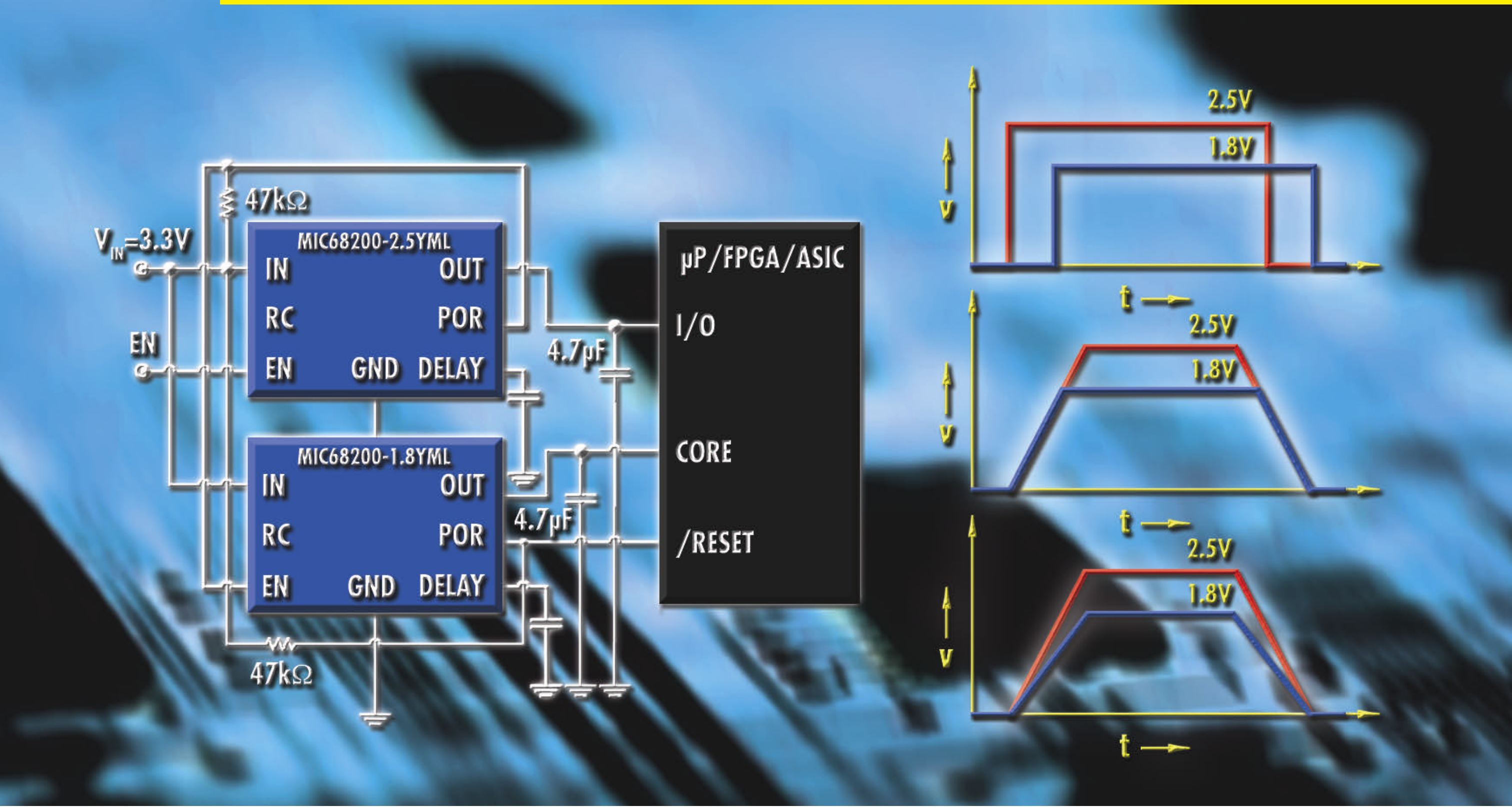

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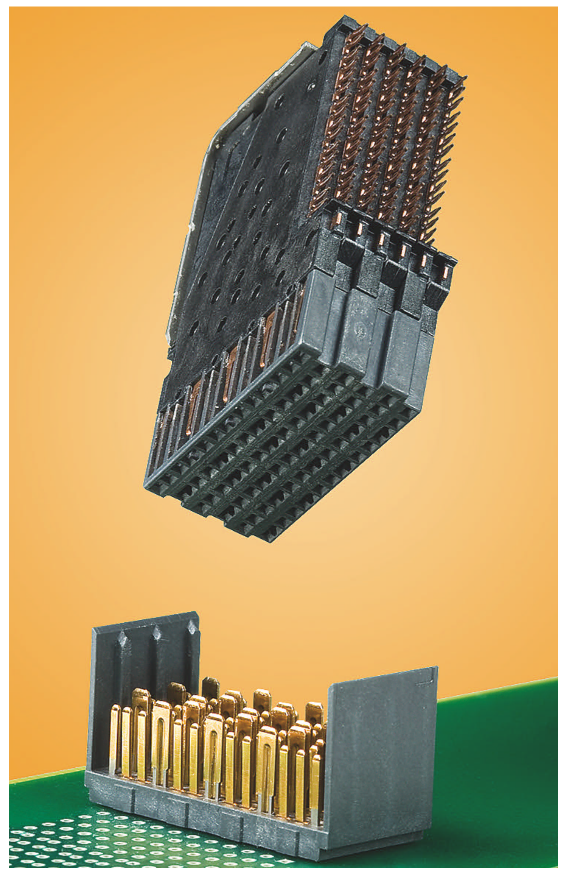
Connector matches PCIe and 10 Gigabit Ethernet data rates

Systems based on serial-interconnect standards, such as PCIe (PCI Express), and networking standards, such as 10 Gigabit Ethernet, invariably need cable and connectors than can handle the escalating data rates. For exactly such applications, Amphenol has announced the XCede connector platform. XCede targets datacom, telecom, storage, and wireless equipment that leverages PCIe and Gigabit Ethernet, along with SONET/SDH (synchronous-optical-network/synchronous-digital-hierarchy), Fibre Channel, and InfiniBand interconnects. The connectors employ a highly reliable press-fit attachment and incorporate a 3-D shield technology that minimizes crosstalk.

Amphenol will develop XCede connectors on a custom basis because the connectors will connect custom backplanes. The XCede platform supports two-pair (27.5-differential-pair/in.) through six-pair (82-differential-pair/in.) versions. The product platform will also include bus-bar power, stacker, cable, and coplanar interconnects. The XCede connector family is now available at prices of 10 to 16 cents per mated signal line in full production volumes.

—by Maury Wright

▷**Amphenol**, www.amphenol-tcs.com.



A press-fit-connection scheme combines with high density and high speed to make the Amphenol XCede connector family a fit for datacom, telecom, and storage systems.

FIRST UNVEILS 16TH ANNUAL ROBOTICS CHALLENGE

Dean Kamen's FIRST (For Inspiration and Recognition of Science and Technology) organization has just announced the challenge for this year's FIRST Robotics Competition (see "Sportslike competition drives science and technology education," *EDN*, Sept 1, 2006, pg 12, www.edn.com/article/CA6363908). The "Rack 'N' Roll" competition will challenge teams of high-school students to build a robot that can place inflatable tubes on pegs on a 10-ft-high rack. FIRST expects more than 32,500 students on more than 1300 teams from around the globe to participate this year. The organization is always looking for engineers to mentor the students in the challenge that can clearly lead kids to a technical career.

Beginning on March 1, the teams will compete at 37 regional events in the United States, Brazil, Canada, and Israel. The season will culminate at the FIRST Championship, April 12 through 14, at the Georgia Dome in Atlanta. The events are free and open to the public.

—by Maury Wright

▶FIRST, www.usfirst.org.

02.15.07

Real-time, 20-GHz-bandwidth DSO takes 50G samples/sec and captures four 200M-sample records at once

Even though it makes Tektronix's DSA72004 (digital serial analyzer), with its 22-psec, 10 to 90% rise time, sound like the ultimate real-time oscilloscope, the headline doesn't tell the whole story. Besides the 20-GHz DSA unit, Tek is rolling out two similar series of 4-, 8-, 12.5-, 16-, and 20-GHz-bandwidth scopes. The lower priced DPO70000 series offers the same bandwidths and channel counts as the DSA series, but the base units provide a less comprehensive—albeit, upgradable—suite of signal-integrity-software tools. All members of both series can acquire more than 300,000 waveforms/sec in the FastAcq segmented-memory mode. All use DSP filters to let you optimize SNR without altering the sampling rate, and all offer an rms-jitter noise floor of less than 400 fsec.

In addition, the company is introducing the P7500 series of 13- and 16-GHz differential active probes. For designers working on ultra-high-speed serial buses, which use multiple differential lanes, the probes eliminate the need to use two scope channels to view one signal, thus enabling a four-channel scope to display activity on two lanes, each comprising two wire pairs. One of these pairs carries signals toward the probe point while the other transmits signals in the opposite direction. Moreover, a flick of a switch—with no relocation of probes on the unit under test—lets you view not only the difference signal, but also the common-mode signal or either signal in the pair.

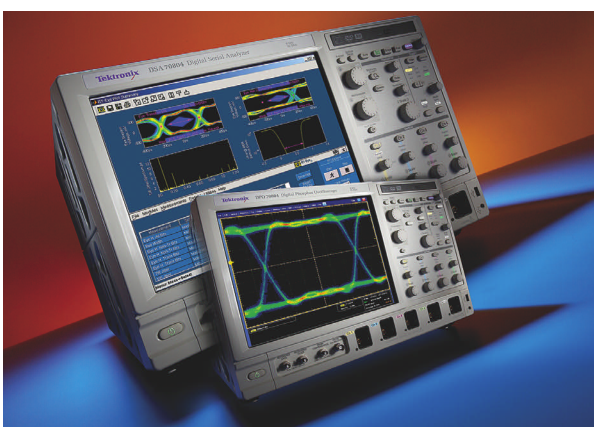
Tek says that the industry now clearly needs real-time scopes with the bandwidth and channel count of the high-end members of these families. Multilane, ultra-high-speed serial-bus data rates are poised to leap forward, and, as voltage swings decrease to enable the higher data rates, compliance testing is proving unacceptable with scopes whose −3-dB frequency is only 1.5 times the data rate—that is, three times the clock rate. The company says that a frequency of five times the clock rate is often necessary and is becoming part of validation protocols that new industry standards prescribe. With devices under development that support data rates of 6.4 Gbps per lane, scopes with a minimum −3-dB bandwidth of 16 GHz on four channels are becoming essential, and the requirement for 20 GHz is not far behind.

The industry also needs scopes with advanced DSP capabilities. You have to know what signals look like where you connect the probes—not somewhere else—and especially not at a point that won't even be part of the device under test once it leaves your lab. Yet, even the best probes require the signal to travel through some length of wire to reach the amplifier input. That trip—even if it's only a few millimeters long—introduces distortion. Fortunately, the wire constitutes a passive, linear network, whose effects you can characterize. A scope with the right computational capabilities can correct for the wire's effects through de-embedding. These scopes can de-embed in real time.

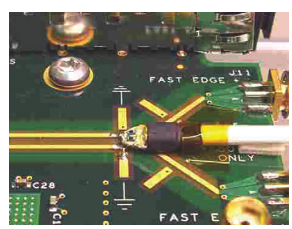
The 12.5-GHz DPO71254 with memory of 10M samples/channel costs $88,500. The DSA72004 with 20M samples/channel—10% of the maximum available—costs $158,000. At the 50G-sample/sec maximum sampling rate, a 20M-sample record represents 0.4 msec. Prices for the P7500 probes begin at $11,000.

—by Dan Strassberg

▷**Tektronix Inc,** www.tektronix.com.

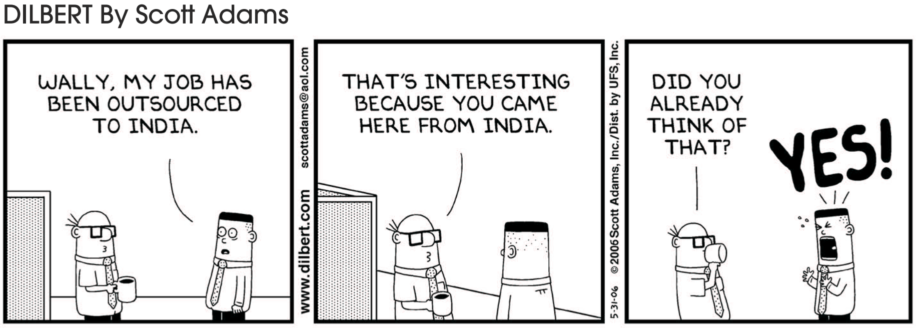


The DSA70000 series and DPO70000 series provide industry-leading real-time bandwidth, a four-channel sampling rate, and memory depth.

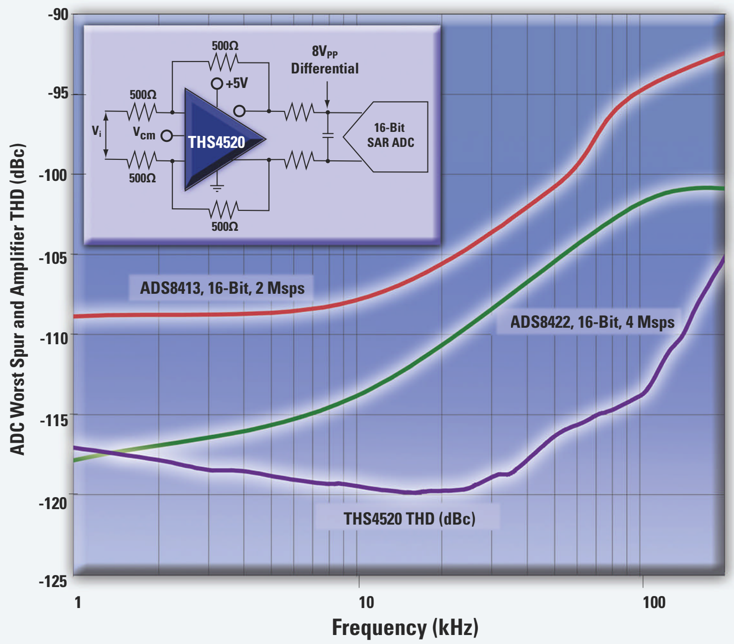


This tiny tip, available on the 13- and 16-GHz P7500-series active differential probes, makes contact with both signal leads and ground, enabling you to display—at the flick of a switch—the differential signal, the common-mode signal, or the signal on either side of the differential-line pair.

DILBERT By Scott Adams



Lowest Distortion, 16-bit Differential ADC Driver



The **THS4520** from Texas Instruments is a wideband, fully-differential op amp with rail-to-rail output. The independent output common-mode control makes it well-suited for dc-coupled, high accuracy data acquisition systems. With its low distortion, the THS4520 is ideal to drive TI's industry-leading, 16-bit SAR data converters.

▶ Applications

- 3.3V and 5V high-resolution ADC driver
- Wireless communication
- Medical imaging
- Test and measurement
- Differential DAC output amplifier

▶ Features

- Rail-to-rail output
- Low noise; $2nV/\sqrt{Hz}$
- Very low distortion:
  - HD2 of –115dBc at 100kHz ($8Vpp$, $R_L = 1k\Omega$)
  - HD3 of –123dBc at 100kHz ($8Vpp$, $R_L = 1k\Omega$)
- Independent output common-mode control
- Power down capability: 15µA quiescent current
- Pin-compatible family of fully differential amplifiers
- Available in a small QFN-16 package

Device	Supply Voltage (V)	GBW Product (MHz)	Slew Rate (V/µsec)	Settling Time 0.1% (ns)	Voltage Noise ($nV/\sqrt{Hz}$)	Supply Current (mA)	Output Headroom (V) (200Ω Load)	Min. Stable Gain (V/V)	THD (dBc)*	Price (1k)**
THS4520	5	1200	570	7.0	2.0	14.2	0.3	1	–92	$2.25
THS4508	5	3000	6400	2.0	2.3	39.2	1.2	2	–101	$3.95
THS4509	5	3000	6600	10	1.9	37.7	1.1	2	–103	$3.75
THS4511	5	2000	4900	3.3	2.0	39.2	1.2	1	–106	$3.45
THS4513	5	2800	5100	16	2.2	41.9	1.1	1	–105	$3.25

** f=10MHz, 2Vpp, 200Ω load*
*** Suggested resale price in U.S. dollars in quantities of 1k*

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www.ti.com/ths4520 ◦ 800.477.8924, ext. 13512

Characterization tool aids SSTA-library creation

To account for process variation while eking out the best mix of performance, power, and yield from new digital-IC-design processes, the IC-design industry is now moving from STA (static-timing-analysis) tools to SSTA (statistical-STA) tools. After years of researching SSTA, companies such as IBM, Cadence, Synopsys, Extreme DA, and Magma Design Automation (www.ibm.com, www.cadence.com, www.synopsys.com, www.extreme-da.com, www.magma-da.com) now offer SSTA tools commercially. But to make those tools work properly requires new timing libraries that account for process variability, not just worst-case-timing estimates. Toward that end, EDA start-up Altos Design has released a library-characterization tool to help foundries, IDMs (integrated-device manufacturers), library vendors, and fabless-IC vendors create their own SSTA libraries for several commercial-SSTA tools.

Altos Design introduced its first commercial offering in July 2006. That tool, Liberate, is for characterizing I/O and standard cells for static-timing libraries and claims runtime improvements over current commercial offerings. Now, the company is introducing Variety, a variation-aware SSTA-library-characterization/modeling tool that generates libraries for various commercial offerings.

The vendors offering SSTA tools also offer characterization tools, but each generates libraries only for its proprietary format. For example, Synopsys' PrimeTime XT SSTA tool uses a new version of Synopsys' CCS (Composite Current Source) format, and Cadence's statistical tool uses Cadence's statistical S-ECSM (sensitivity-based effective-current-source-model) format. Similarly, IBM, Magma, and Extreme DA have their own formats.

Jim McCanny, Altos' chief executive officer, says that Variety, as its name implies, will generate libraries for many of those vendors' formats and will do so faster than each vendor's characterization technology. "With Variety, users will be able to generate libraries that account for both systematic and random variation," says McCanny. "Other tools take a black-box approach. We don't do that. We try to understand the circuit. We understand the functions, what vectors are required to sensitize, what paths there are; we do a transistor-level preanalysis of the circuit."

> "Systematic variation is relatively easy to characterize, whereas random variation tends to be more complex.

Whereas models for STA tools capture worst-case cell performance, Variety SSTA models characterize each transistor in a cell and account for both systematic and random variation. The tool generates SSTA models with nominal timing information plus additional data representing the impact of any number of parameter variations. McCanny notes that systematic variation is relatively easy to characterize, whereas random variation tends to be more complex. He says that a typical systematic variation is a shorter gate or trace length. "If, for example, a length shrinks by 5%, we can characterize it and calculate the sensitivity of the delay to that change of length," says McCanny. When users add a systematic variation to the characterization, it typically adds one times the runtime to the tool.

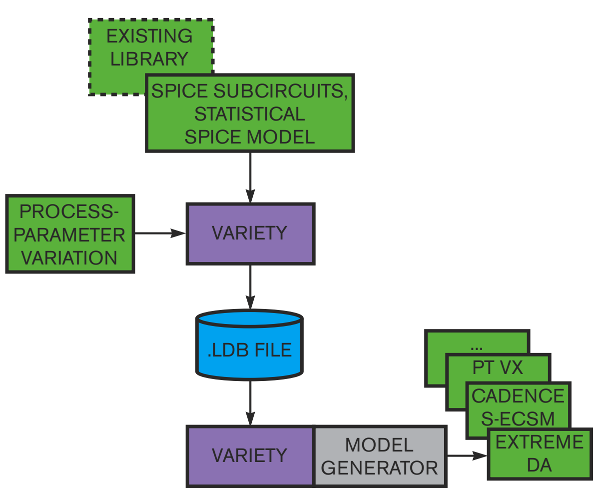
Characterizing random variation is a bit more challenging. "With random-variation characterization, we model the effect of a parameter on each unique transistor in a cell," he says. "An average standard cell has 25 transistors per cell, so if you did this with a black-box method, you would end up requiring about 25 times more characterization effort. That's impractical, so what we do is to reduce that 25 times to somewhere around two to three times."

The tool employs an algorithm that quickly locates the transistors that a user-specified random variation will affect. "You can model any Spice parameter you have in your model: low- or even high-level parameters you created from a combination of physical parameters," says McCanny. Users can add any number of variations to the characterization runs. He notes, however, that, each time users add a random-variation parameter to the tool, it increases the runtime by a factor of three.

Renesas (www.renesas.com) has benchmarked the tool's modeling length, width, and thermal oxide as systematic variations and has benchmarked threshold voltage as a random parameter. The tool characterized 387 cells in six hours on an eight-CPU system. It characterized nine systematic variations and one random variation in 27 hours on a 16-CPU system.

Variety creates libraries in its own .lbd database format and then translates the file into ECSM, CCS, or Extreme DA's internal format, with other formats to follow. That translation allows users to use the same

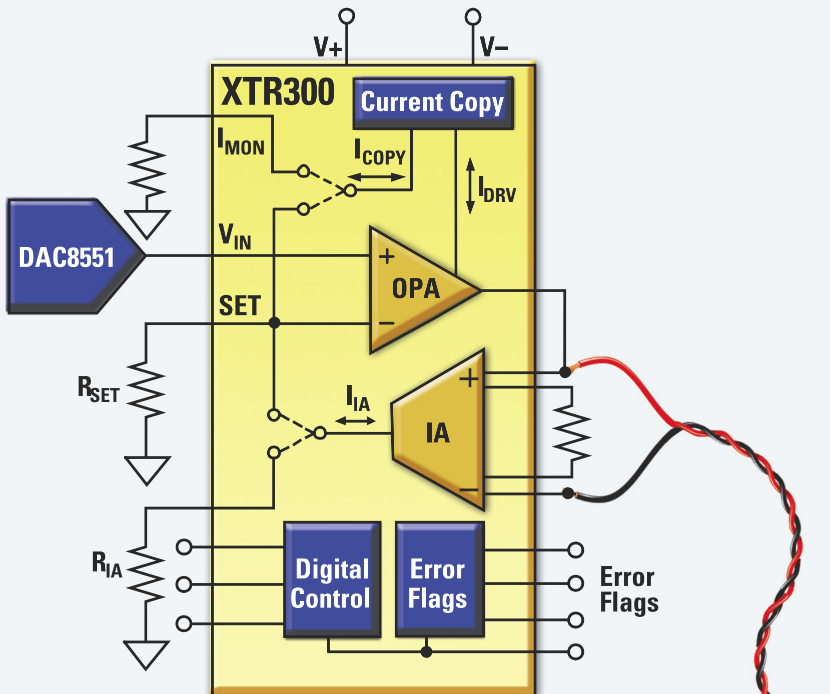
(continued on pg 28)



Altos' Variety supports multiple SSTA tools.

Versatile Industrial Output Driver

Voltage or Current Output



Burr-Brown Products from Texas Instruments

Applications

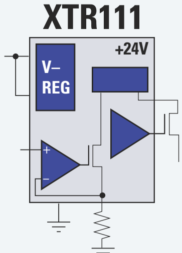
- PLC output programmable driver
- Industrial cross-connectors
- Industrial high-voltage I/O
- 3-wire-sensor current or voltage output
- ±10V 2- and 4-wire voltage output

Features

- User-selectable: voltage or current output
- Supply voltage: up to ±20V
- V_{OUT}: ±10V (up to ±17.5V at ±20V supply)
- I_{OUT}: ±20mA (linear up to ±24mA)
- Short- or open-circuit fault indicator pin
- No external current shunt required
- Over-current protection
- Separate driver and receiver channels
- Package: QFN-20, TSSOP-20 coming soon
- Price: $2.45 in 1k units

The new **XTR300** from Texas Instruments is a complete output driver for industrial PLC and process control applications. Its digital I/V select pin allows the output to be configured as current or voltage. The device features error flags and monitor pins to provide a high level of diagnostic system checks, and make remote configuration and troubleshooting possible.

XTR111



NEW

The new **XTR111** is an output driver for 0-20mA or 4-20mA from a standard voltage input. It can also be connected for voltage output. It operates from 24V (up to 40V) and provides an adjustable voltage regulator output, output disable and a load error flag. Price is $1.45 in 1k.

Industrial Solutions Guide
Datasheets, Samples and Evaluation Modules

www.ti.com/xtr300 ◦ 800.477.8924, ext. 3681

Technology for Innovators™ Texas Instruments

(continued from pg 26)

library with any of these vendors' tools. McCanny notes that it will be especially useful for design groups who use one vendor's SSTA tool for design and then use another vendor's SSTA tool for sign-off. Characterizing libraries in Variety allows both tools to work from the same library.

This neutrality has led Altos to offer Variety to the Si2 (Silicon Integration Initiative, www.si2.org) to help the organization's OMC (Open Modeling Coalition) derive an industry-standard reference flow for library characterization, modeling, and model usage. The Si2 will install Variety into OMC's reference flow as the characterization subsystem for statistical characterization of library data. As part of the reference flow, Altos will help the OMC define standards for library-flow interfaces for communicating statistical information between elements in the flow.

Variety's entry price is $95,000, and prices for a typical system start at approximately $250,000 for a one-year subscription. The tool currently supports Cadence's and Extreme DA's SSTA tools, and Synopsys' tools will soon follow. The company hopes to later add support for Magma's and IBM's SSTA tools.

—by Michael Santarini

▷**Altos Design Automation**, www.altos-da.com.

Laptop power efficiency increases in dribs and drabs

Pity the poor laptop designer: Because laptops—or, by extension, any piece of portable equipment that uses a power-hungry Intel-type processor—must operate seamlessly from either an ac power adapter or a battery, the system-power circuitry must support a load that can vary from slightly less than 9V to slightly less than 17V. When you plug the laptop into ac power and the system is sucking juice from the adapter, dc voltage can range to a typical high of 16.8V. But when the laptop is running off battery power, dc voltage can be as low as 8.7V. Because the system must support such a wide voltage range, the power losses are heavy: Switching losses increase at higher voltages. Plus, the dc/dc-switching frequency and, thus, efficiency are lower at higher voltages.

Intel officials realize that, if system architects seek to increase system speed and capability simply by following the current system-design methodology of cranking up clock speeds, laptop operating temperatures will shortly approach the surface temperature of the sun with a corresponding battery life in the milliseconds. So, the chip giant over the years has introduced a number of guidelines for improving power efficiency through system architecture. Enter Intel's NVDC (Narrow Voltage DC) initiative, which seeks to lower power losses by shrinking the system-load range. The strategy calls for replacing the battery-charger circuit with a system-level charger-voltage regulator, dropping the load the adapter sees to 12.6V from the current 16.8V.

Majid Kafi, director of Intersil's Notebook Power products group, sees it this way: "This [approach] supports the battery [voltage] as powering the system bus, and it requires a much smaller voltage range than traditional power schemes in the notebook." The total impact is 2 to 3% better efficiency. These numbers are not eye-popping, but squeezing out more system-power efficiency occurs in dribs and drabs. For laptops with the highest power density batteries, this increase can result in as much as 30 extra minutes of runtime.

Are laptop manufacturers jumping all over NVDC? Not yet: Kafi says that one major OEM has switched to it, but the vendor has made the commitment of basing all its new notebook lines on it, and Kafi sees this indicator as an industry trend. Intersil is hoping that's the case: It has just introduced the ISL6257 NVDC battery-charger controller, which Kafi believes is the first NVDC controller to reach the market. As laptop manufacturers see that there is no silver bullet—no new battery technology that will appear in the near future—picking up power efficiency in dribs and drabs will have to suffice. (That's right: Don't hold your breath for cost-effective, energy-dense nanotechnology or micro fuel cells.)

—by Margery Conner

▷**Intel**, www.intel.com.

▷**Intersil**, www.intersil.com.

FEEDBACK LOOP

"I relish my vacations in New England and the Adirondacks, where Internet connectivity is often nonexistent or measured in HBS (hundreds of bits per second)."

—D Wiesen, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6406715. Add your comments.

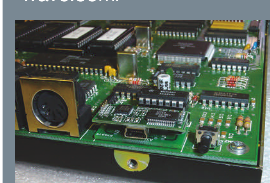
02.15.07

USB MODULE REPLACES LEGACY RS-232 CONNECTORS

Do you need to add USB support to a product that includes a serial port and a DB-9 or DB-25 connector? Well, you could redesign the pc board and add a USB chip and connector, or you could simply replace the DB connector with Timewave's RS-232-To-USB Conversion Module. The module fits directly into the DB-connector footprint, interfaces with the serial-port signals, and externally presents a USB interface. The design is USB 2.0-compliant, although it supports only 12-Mbps full-speed operation. Timewave supplies Linux and Windows drivers. Available now, the modules cost $79.95 each.

–by Maury Wright

▶**Timewave**, www.timewave.com.



A USB module that fits into the footprint of a DB-9 or DB-25 connection provides a quick retrofit for products that need USB connectivity.

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ANALOG DEVICES

IC-tool flow supports new power standard

Cadence Design Systems is moving full steam ahead with its controversial CPF (Common Power Forward) power-analysis format with or without industrywide acceptance. The company recently announced that just about its entire IC-design flow includes new low-power-design technology that it built with the format. The company last year announced its PFI (Power Forward Initiative) and its intention of working on CPF efforts, but it did not invite any other EDA players to help define the format. The lack of openness caused competitors Mentor (www.mentor.com), Synopsys (www.synopsys.com), Magma (www.magma-da.com), and a few other EDA companies and customers to form an alternative effort, the UPF (United Power Format), a seemingly more open effort under standards body Accellera (www.accellera.org). Cadence caved in to the pressure and last summer allowed a half-dozen or so smaller EDA companies offering power-related technologies to join the effort—but still not define it—as "advisors." It also sped up the timetable on donating CPF to a standards body, Si2's (www.si2.org) newly formed LPC (Low Power Coalition), and getting LPC- and PFI-member companies to approve the first specification of CPF.

Cadence has maintained all along that it developed the format in an arguably "closed" fashion so that it could avoid all the bureaucratic slowdowns associated with standards development. Critics have argued that Cadence was moving ahead with its own standard when the industry had viable working alternatives simply to introduce a front-to-back low-power flow before anyone else did. It turns out that both Cadence and its critics are correct: Cadence indeed went from raw specification to what the company claims is a workable format in less than a year, and it now has tools.

"You don't design chips with formats; you need an EDA system to do it," says Eric Filseth, Cadence's corporate vice president of product marketing. "We now not only have a format that works, but also the tools that use that format to help customers get a handle on low-power-design problems." Filseth notes that the PFI-member companies received the tools last quarter and are using them in production-design projects. This release will likely be the turning point that will make the industry start to embrace the format, he notes.

The latest version of Cadence's Encounter implementation-tool lineup, Version 6.2, and the latest version of Incisive, Version 6.0, which Cadence released last month, all will include technology to help users better create low-power designs. Cadence users will be able to define power parameters at the RTL (register-transfer level) and do what-if analysis during synthesis to ensure that their IC designs will conform to power specifications in each power mode of operation. Implementation tools will then be able to place and route the design based on the format. If a specification needs adjustment, its potential impact will be traceable at each phase in the IC process: RTL, synthesis, and physical design.

> "In the past, lots of manual work was required to transfer this data around and translate it, and that brought with it mistakes."

"You specify your power strategy once at the beginning of the design flow, and the rest of the EDA system follows it and knows what to do with the data it gets. It all comes off the same data format, so you can simulate the layout," says Filseth. "It benefits productivity because it is more automated and integrated. In the past, because there hasn't been ways of representing all this data, lots of manual work was required to transfer this data around and translate it, and that brought with it mistakes." Cadence still has a bit of work to do to ensure that the entire Cadence flow works from the format. For example, Cadence emulators do not yet support CPF, but its digital-design, software-verification, and implementation tools do.

Jan Willis, senior vice president of industry alliances at Cadence, hopes to see the UPF members eventually embrace the CPF under the Si2. For now, however, users employing a mix of third-party tools, as most do, must manually translate some of the power information from CPF into the third-party tool's power format—if it has one—to get a workable flow. The other CPF-member companies are expected in the coming months to announce that their technologies also run on the CPF format, because Cadence this month released a parser for CPF.

Filseth notes that, if another low-power standard does eventually prove to be better or becomes the de facto standard, Cadence will likely support it, too. For now, the idea is to get a workable product in customers' hands. Coming out with a tool long before the format has industrywide acceptance is Cadence's attempt to shrink the gap—and get a jump on the competition.

—by Michael Santarini

▷**Cadence Design Systems**, www.cadence.com.

FEEDBACK LOOP

"I worked for GE Space System Division in Valley Forge, PA. There was nothing quite so interesting to do for lunch one day a month other than to go over to the surplus warehouse where employees had first crack at all kinds of office furniture to electronic and scientific equipment, before the professional vultures were let in."

—Anonymous, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6406727. Add your comments.

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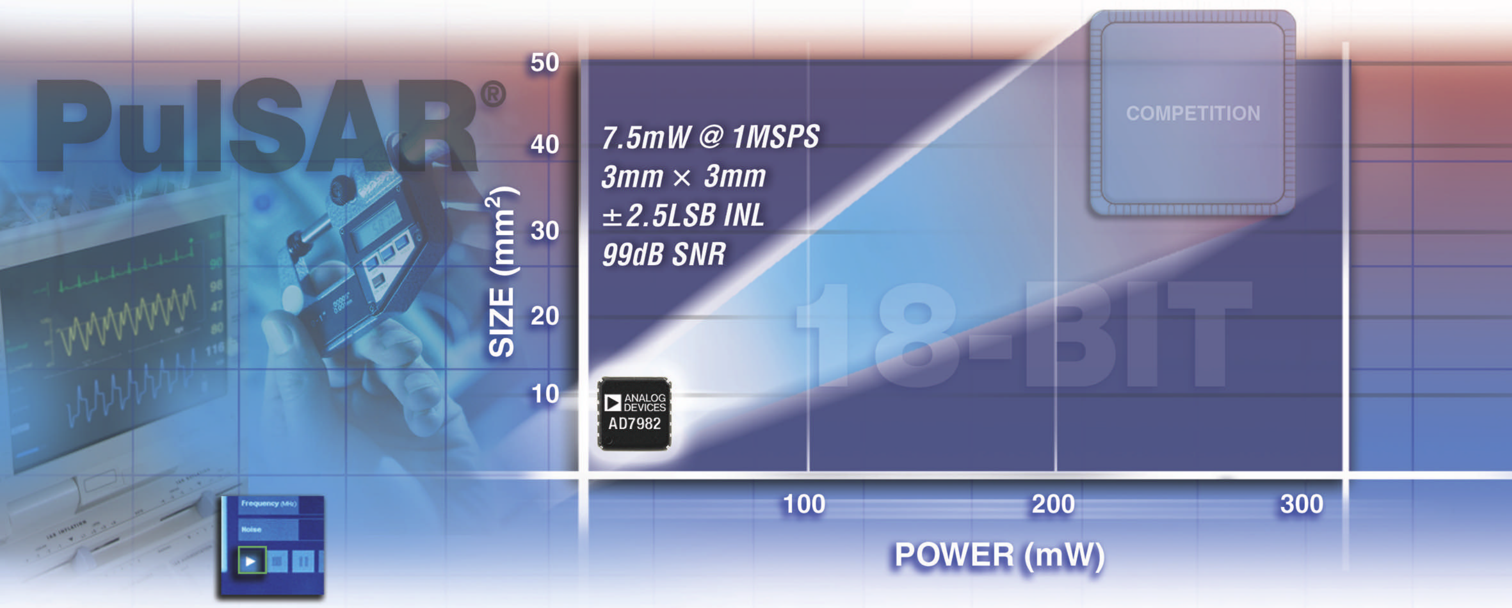

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Recommended ADC Drivers

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Part Number	Resolution (Bits)	Sample Rate	Max Integral Linearity (LSB/ppm)	SNR, noise rms (dB/ppm of FSR)	Power @ 100 kSPS	Price ($U.S.) @ 1k
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AD7690	18	400 kSPS	±1.5 LSB, ±6 ppm	102 dB, 2.8 ppm	4.4 mW	19.50
AD7691	18	250 kSPS	±1.5 LSB, ±6 ppm	102 dB, 2.8 ppm	4.4 mW	14.50
AD7980	16	1 MSPS	±2 LSB, ±30 ppm	91.5 dB, 9.4 ppm	750 µW	19.50
AD7693	16	500 kSPS	±0.5 LSB, ±8 ppm	96.5 dB, 5.3 ppm	3.6 mW	18.00
AD7685	16	250 kSPS	±2.5 LSB, ±38 ppm	93.5 dB, 7.5 ppm	1.35 mW	6.50
AD7942	14	250 kSPS	±1 LSB, ±61 ppm	85 dB, 20 ppm	1.25 mW	4.75

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ANALOG DEVICES

VOICES

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Craig Lund is vice president and chief technology officer at Mercury Computer Systems (Chelmsford, MA, www.mc.com), a leading provider of computing systems and software for data-intensive applications, such as image processing, signal processing, and visualization. Lund leads Mercury's Technology Office in search of breakthrough innovations and disruptive technologies. He holds a bachelor's degree in engineering from the University of Connecticut (Storrs).

As you look to the 2007 and 2008 time frame, what technologies offer the biggest opportunities for designers?

A I believe things like the changes in the standard base, the emergence of multicore processors, and the advent of acceleration technologies represent potential discontinuities. Every time there is a discontinuity, there is an accompanying opening for new winners and losers. I don't mean just for companies. Inside a company, new people will be recognized as key employees because of their expertise in the "new thing." I'm sure the winners will all be avid *EDN* readers.

With the proliferation of standards from VITA [VMEbus International Trade Association], PICMG [PCI Industrial Computer Manufacturers Group], and others, plus the competing switch-fabric technologies, how does the COTS [commercial-off-the-shelf] industry prevent fragmentation and interoperability problems?

A Innovation comes first. Experience is second. Standardization follows. What is happening today within VITA and PICMG is that people are skipping the middle step, jumping from innovation directly into standardization. The label "industry standard" has lost its historic association with the characteristics "mature and low risk." Today, standard really means "formally documented and available for others to experiment with."

The Darwinian marketplace has not changed, just the vocabulary. Salesmen might tell you their offering is "industry-standard," but buying a bleeding-edge standard or technology is always a little risky. Experience—the passage of time—is the only guaranteed way to fix that. Mercury has an enviable record of picking winners, so, if you need to take technology risk, you should at least put us on the list of folks with whom to consult. To answer you directly, I believe the industry will be faced with interoperability challenges for some time still.

Multicore processors are currently pushing the technology envelope. What resources does it take to harness that computing power for future embedded products?

A The microprocessor suppliers rarely emphasize the downside: that a single thread of execution is no longer getting faster. Instead, they emphasize the fact that we are getting more and more threads each generation.

How many consumer applications can exploit dozens of threads? After maybe eight threads, I believe that multicore architecture will become a niche technology focused at transaction-processing servers. My bold prediction is that everything else will migrate to look a lot like a Mercury multicomputer on a single chip. This [approach] is the only way to make a single thread of execution go faster: by deploying specialized computing elements tuned for a particular task. The first such example was the GPU [graphics-processing-unit] chip, a device designed to accelerate OpenGL and DirectX libraries. The second example is the Cell Broadband Engine, a device designed to make game-physics libraries run faster. TCP/IP [Transfer Control Protocol/Internet Protocol] Offload Engines are a third example of specialized hardware used today to make portions of a single thread run faster.

If I am correct, the low-level programming challenge inside these chips will be choreographing the flow of data blocks between the various processing-element flavors. This [idea] is a self-serving view of the future as I'm predicting Mercury's skills and know-how become more valuable over time. However, if I did not believe, I would not be working here.

What are the biggest technical challenges or bottlenecks that you face in the high-performance-embedded-systems industry?

A You asked specifically about "high-performance" systems. Here, in addition to the standards and multicore issues, we face another challenge: There are fewer microprocessor options available each year. The choices we do enjoy tend to consume far more power per square inch than most embedded systems tolerate. More abstract, but equally annoying, is the fact that peak performance is rising much faster than memory bandwidth, leaving real-world applications memory-bound. There is an upside to the memory-bandwidth challenge: Any high-performance system that you acquire today will likely have a longer life span than previous acquisitions because there will be less pressure to upgrade every time a new processor is announced.

You can also work around the memory-bound challenge by exploiting processors with unusual memory architectures, specifically Cell chips, GPU chips, and sometimes FPGAs.

—by Warren Webb

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Windows Embedded

BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

The Miller's tale

It is noteworthy that, despite the vast breadth of our industry, its myriad applications, and its diverse technologies, the fundamental building blocks we use in electronic circuits are remarkably consistent and small in number. This observation, pedestrian perhaps at first glance, is eye-opening when you consider that our collective interests span a spectrum from dc to daylight, cover dissipations from flea power to horsepower, and target environments from human-body implants to deep space.

The expectation that a handful of part types should meet such disparate requirements is akin to one that would have paper clips and staples as integral components of trestle bridges: Few things scale to such an extent as do electronic devices. As a result, familiar bipolar and field-effect transistors, a few related active devices, and a whopping three types of passives—resistive, inductive, and capacitive—account for most of our components, no matter if we mount them as discretes on a pc board or construct them in a solid-state fabrication process.

The diversity of our circuits originates not, then, with the number of distinct components at our disposal—each deriving its behavior from unique physical principles—but rather from topological inventiveness. Historically, this small number of distinct part types has been an advantage: Designers could familiarize themselves with the behavioral nuances native to each type and craft elegant circuits that took best advantage of their constituent elements.

As system complexities and functional densities have grown, however, many designers find themselves engaged in design practices that are, by necessity, far removed from those underlying physical principles and from the behavioral nuances of individual devices. Yet it is those individual devices—by handfuls, hundreds, thousands, or millions—and the interactions imposed by the topology they inhabit that determine your product's performance. As a result, certain device-centric themes appear in widely varying contexts.

One of these themes is the Miller capacitance—a feedback element implicit to active devices as different in their operating principles as bipolar-junction and field-effect transistors. The Miller capacitance does not appear explicitly as a parasitic in the active device's small-signal model; you can calculate it from the model and from the electrical conditions that the surrounding circuit imposes as the effective impedance between the internal base node and the collector or between the gate and drain.

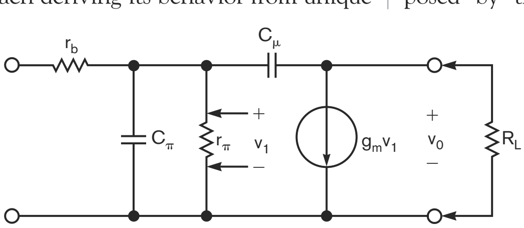

Figure 1 This small-signal bipolar-junction-transistor model includes the output load connection for a common-emitter amplifier configuration.

Using the bipolar-junction transistor's small-signal model as an example (**Figure 1**), the magnitude of small-signal transconductance, g_m, derives from the ratio of the collector current and the thermal voltage, kT/q, where k is Boltzmann's constant, T is the temperature in Kelvin, and q is the electron charge. The base-collector capacitance, C_μ, results from the base-collector depletion layer and is a nonlinear function of the voltage across that junction.

Assuming a common-emitter configuration, Kirchoff's current law at the output node yields

$$(v_o - v_1)C_\mu s + g_m v_1 + \frac{v_o}{R_L} = 0.$$

Because the current through the base-collector capacitance contributes negligibly to the load current, a good approximation of the output is

$$v_o = -v_1 g_m R_L.$$

Finally, calculating the impedance between the internal base node and the collector yields the Miller capacitance:

$$\frac{v_1 - v_o}{i_{C\mu}} = \frac{v_1(1+g_mR_L)}{i_{C\mu}} = \frac{1}{C_\mu s}$$
$$C_{MILLER} = (1+g_mR_L)C_\mu.$$

Though the C_μ depends on the transistor's physical attributes and dc bias, the small-signal Miller capacitance is larger by a factor of one plus the stage's gain—g_mR_L—the result of the interaction between the device and its electrical surroundings. **EDN**

Contributing Technical Editor Joshua Israelsohn is director, technical information for International Rectifier. Contact him at edn-joshua@sbcglobal.net.

BY BONNIE BAKER

Engineers need stories, too!

Now that another year has wound down, the deluge of hotel technical seminars for 2006 is finally over! Attendees came from near and far to hear what vendors had to say about their wares. It's true; I can get a lot of this information off the Web. So, why do I go to these seminars? Because I want to become excited and delighted with new ideas that, in the end, will make my job easier. If the presenter tells me a good story about his or her products, techniques, and experiences, it may help me to look at my problems through different eyes.

Granted, not all seminar sessions hit the mark, and I have seen a variety of hotel seminars. Some presenters stand proudly and read their slides. (I can read, thank you very much!) Some whip through their material with a dry, just-present-the-data delivery, similar to Joe Friday from television's *Dragnet*: "Just the facts, Ma'am." I have seen presenters that go so far as to be funny and entertaining, as well as knowledgeable, but they never quite do the trick, either. With this type of presentation, I never get answers. I leave with the same set of tools and techniques I came in with, except now I have a few new jokes to tell at work. Argh!

The type of seminar that I enjoy and remember the most is when the presenter essentially tells me what he will talk about, points out why his topic is important, comprehensively covers the material, and summarizes with the original objective. Couching these four points in a story line goes a long way to pull the presentation together. This format may sound uninspired, but the icing on the cake is when a speaker injects pertinent stories throughout the presentation. This type of organization provides attendees with packets of sensory material that the listener can quickly and easily internalize. These presentations are true to the engineer's heart, packed with actual experiences, and void of marketing hype.

If the presenter tells me a good story about his or her products, techniques, and experiences, it may help me to look at my problems through different eyes.

So again, with all of the material out there—articles, Web seminars, podcasts, and so on—why do engineers still come to these face-to-face seminars? I wish you could see my face as I tell this story. At one point in my career, I had a manager tell me that we didn't need to train our seminar presenters; he did not want to spend money to fly them to the training session. Can you imagine my reaction? I looked like a deer in the headlights. I was stunned! In response to this misaligned cost-cutting measure, I calmly stated, "You are right. The speaker has little influence on the seminar, anyway. As a matter of fact, let's just package up the books and mail them to customers so they can read the material at their leisure. Then we can cancel the seminar's hotel arrangements and the speaker's plane tickets. Doing so will save the company a lot of money!" Well, luckily, we did have training that year for the seminar presenters. And you should have heard the stories the presenters told on the road!

Many times, engineers attend these hotel seminars to get the inside scoop. In fact, I know engineers who travel across the country to see and hear the voice of the presenters that work at their corporate home base. These technical presentations usually have an abundance of undocumented tips and tricks. As you may know, in the business world, location is everything. But, in the seminar world, presence has much more value.

So, before you step in front of an audience, whether it is in a hotel conference room or in one of your company meeting rooms, know your story before you walk into the room. Have in mind the beginning, middle, and end, as well as anticipated questions. This strategy gives you a credible start when you set out to portray confidence to the masses.

So … what is your story? **EDN**

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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 BY LYNN SMITH

In the days of old, when engineers were bold

DANIEL VASCONCELLOS

In the 1970s, around the time that MOS Technology introduced the 8-bit 6502 processor, I took a job as chief engineer at a company that developed, manufactured, and supplied military and industrial security-monitoring systems. Job 1 was an intermittent problem in the current model that caused the watchdog timer to reset the system. The default condition for a system reset was to secure all doors and sensors throughout the monitored areas to condition "red." Then, when a normally "green" door opened, alarms sounded. This problem was a particularly disturbing one because this equipment was monitoring sensitive areas, such as nuclear-storage facilities in which the false alarms could cause response teams to react.

The 6502-based equipment had the usual ROM, RAM, I/O, and a built-in small Seiko line printer (**Reference 1**). In those days, we tried to make one little processor do everything; why not? Popular theory at the time was "it is a hardware problem," and there was good reason to believe it. First, the design was poor and had mixed-logic families on a poorly laid out bus. It also had some ground bounce, because these were the days before multilayer boards were common. Worst of all, we were just learning about the "dirty dozen," 12 illegal instructions for the 6502 that, if executed, would cause the processor to halt. We used to call it "halt and catch fire"; some of these instructions required a power-down and backup to clear. After three months of many ECOs (engineering-change orders) to correct all the hardware deficiencies, the problem had not changed at all in nature. Now, with solid hardware, we were really scratching our heads.

There was one thing about the design that rubbed me the wrong way right from the beginning: the fact that the little Seiko line printer was tied to the NMI (nonmaskable interrupt). The 6502 controlled the printer, and the NMI monitored the synchronous pulse from the printer. Now that hardware was looking good, there was some finger-pointing over whether the problem now was hardware or software. After many hours in the lab and reports from customers, we narrowed the behavior for the intermittent failure as occurring only after the printer was winding down from printing.

After yet another long day in the lab, the NMI was still bothering me, especially now that I knew that the printer was involved. I began thinking about the 6820 PIA (peripheral-interface adapter) and the initialization sequence; then, it hit me. It was so simple: The 6820 PIA takes two instructions executed in sequence to initialize it. You cannot interrupt the instructions. I drove back to the office, and the software guys were still there. I checked, and, sure enough, when the printer was done printing, they went out and reinitialized the PIA just for grins!

For me, it was so obvious and "case closed." The short story is that I had them take out two lines of code, and we never saw the "hardware" problem again. The long story is that management and software people spent many more days testing because they just could not believe it. After much more testing, the senior programmer and I flew to one of our main problem locations and installed two new ROMs; no further problems occurred. EDN

REFERENCE

1 http://en.wikipedia.org/wiki/MOS_Technology_6502.

Lynn Smith was a consultant and hardware engineer in Silicon Valley for 30 years before recently pulling up stakes in San Jose, CA, to move to Alabama, where he is building an airpark. Like Lynn, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

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Visit www.edn.com/070215pry for a more in-depth description and additional photos of our deconstruction of the Spaceship Blaster—as well as three other cereal-box toys.

See inside a cereal surprise

Microsoft continues to deny rumors of a handheld Xbox game console, but the company did recently promote its Xbox brand by including a series of Mini Games in boxes of Kellogg's cereals. How did the designers deliver a compelling user experience when their end product had to be inexpensive enough to give away in a box of Froot Loops or Frosted Flakes?

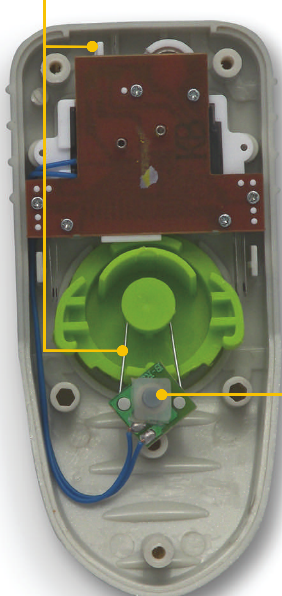
The power switch and front-panel knob connect to the single-layer pc board through proximity-improvised contacts, preserved by six tiny screws. The membrane switch tethers to the board using a more conventional wire-and-solder approach.

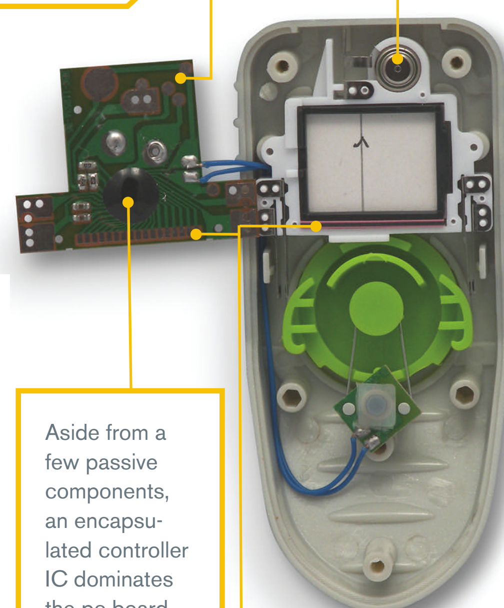
The on/off switch is crude but effective, as are the dual contacts on either side of the control knob, which sense clockwise and counterclockwise twists. A tension wire returns the knob to its neutral position after release.

Two spring-loaded contacts press against and electrically stimulate the low-fidelity speaker.

A membrane switch communicates that the user has activated a button on the back of the game.

Although the designers expect users to discard the Spaceship Blaster game once its battery gets depleted, intrepid tinkerers can replace the power source if they can get past the non standard screws holding the case together.





Aside from a few passive components, an encapsulated controller IC dominates the pc board.

Display-driver contacts lining the bottom edge of the board mate to the low-resolution monochrome LCD, beneath the reflective backing cover shown, using a "zebra strip"—an elastomer that embeds alternating bands of conductive and insulating material.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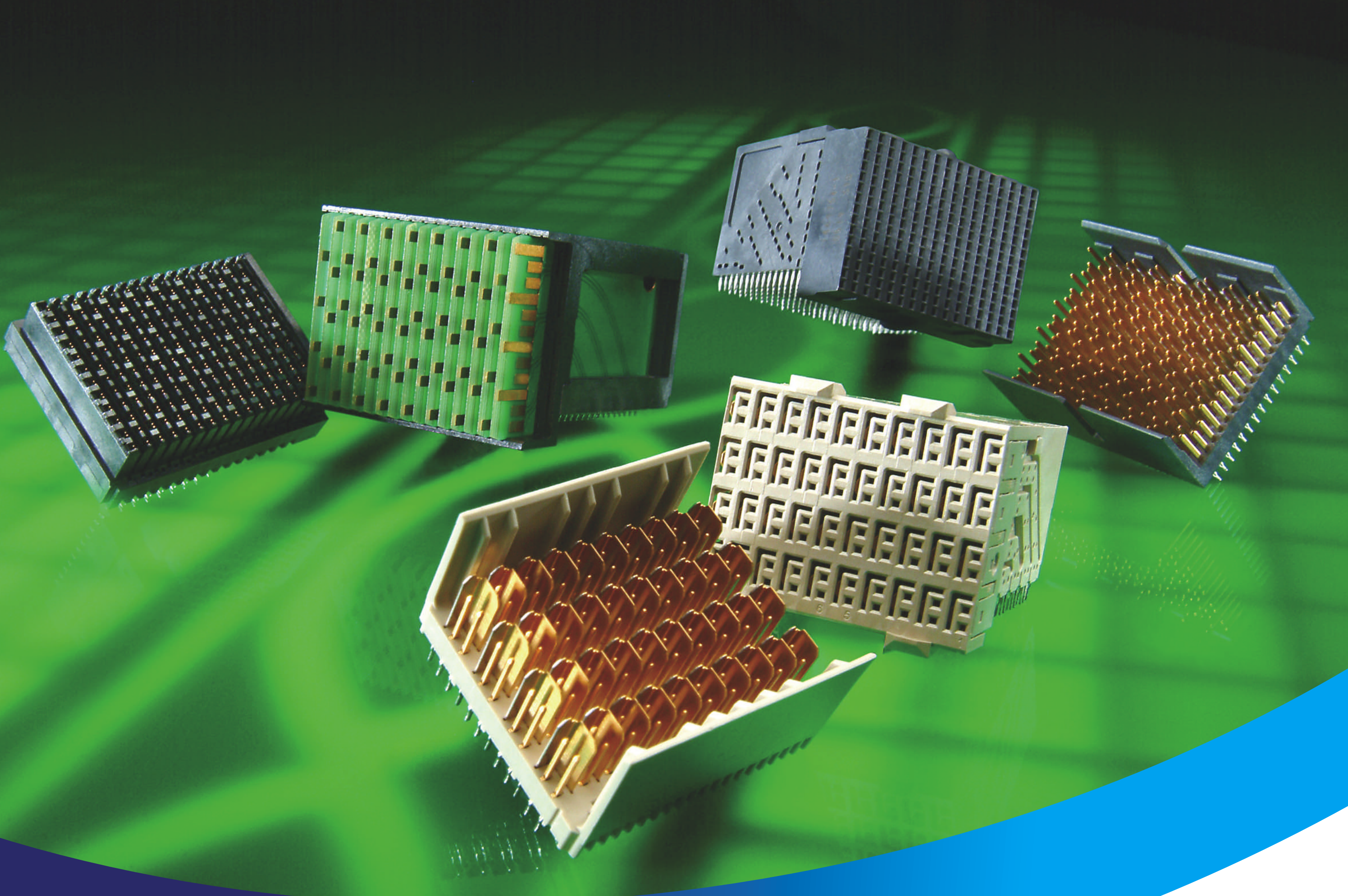

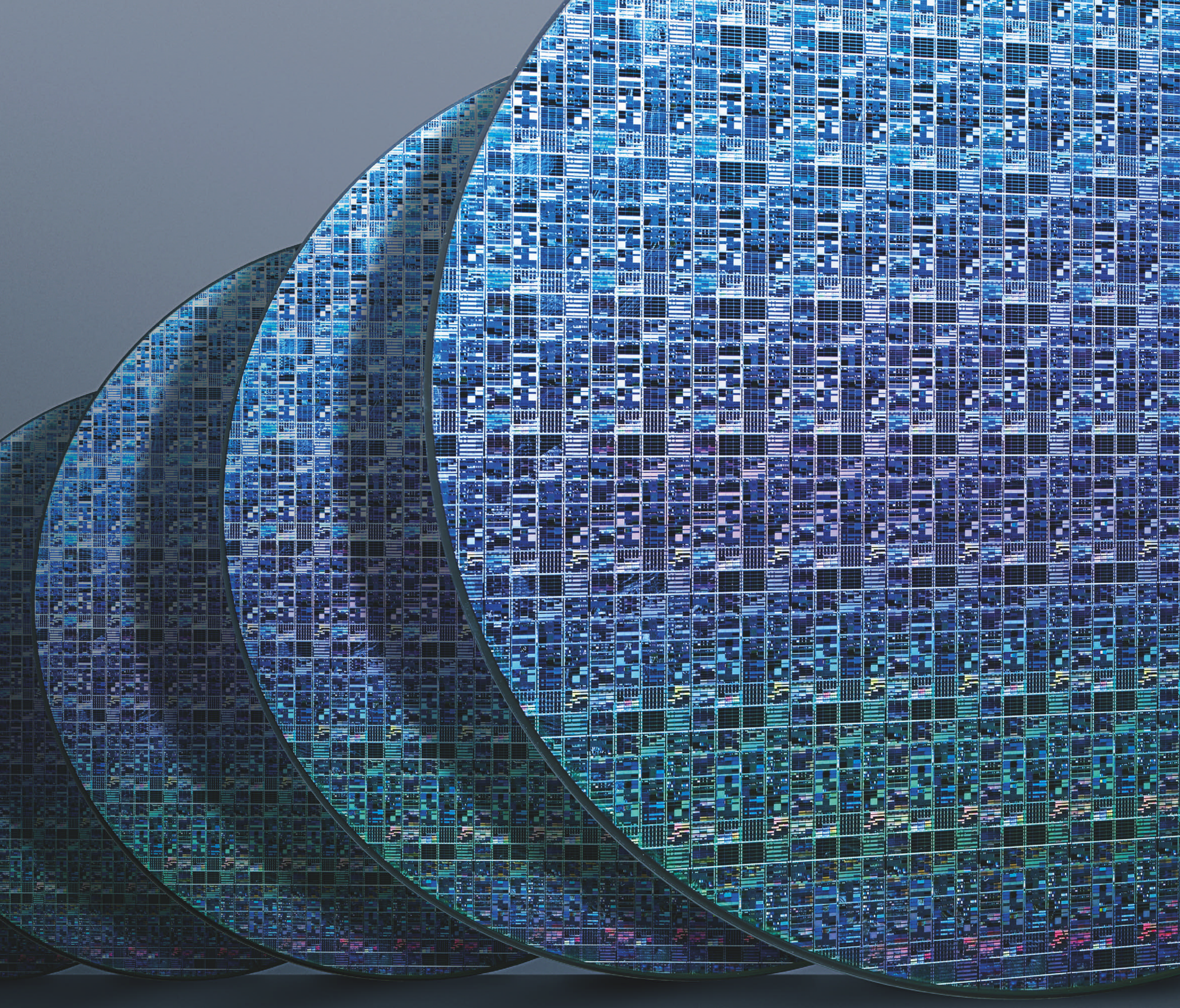

ANALOG edge[SM]

Techniques for Thermal Analysis of Switching Power Supply Designs

Application Note AN-1566

Frederik Dostal, Applications Engineer

To reduce time-to-market and component count, power management ICs with integrated power transistors such as National's new SIMPLE SWITCHER® regulators (LM5576, LM25576, and others) are often preferred over controllers with external FETs. However, with the power transistor on-board, it's important to do careful thermal analysis of the power IC to make sure the silicon temperature does not exceed the maximum allowable junction temperature. Integrated circuits are rated up to a maximum 'die' temperature. Operation at higher temperatures will put the IC out of specification and possibly destroy it.

There are three main ways of thermally analyzing a given design. The following article explains the different approaches, and discusses the precision of each approach.

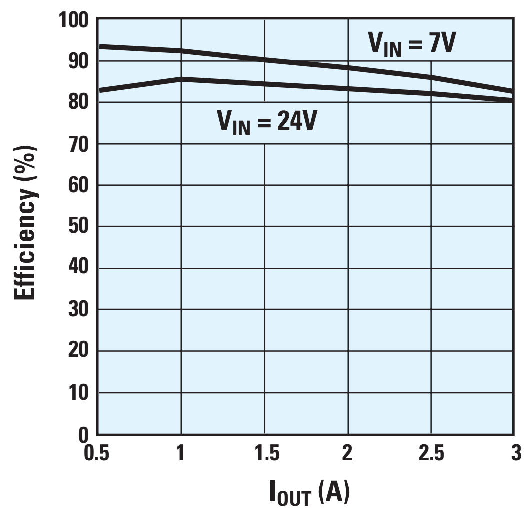

Figure 1. Typical Efficiency at 5V V_{OUT} vs I_{OUT} and V_{IN}

The Analytical Approach

The analytical approach is a good way to get a rough estimate of the die temperature of a given switching regulator. One approach is to calculate the losses the switching regulator IC generates. For step down regulators the following formulas can be used.

There are bias losses which are mainly the ground pin current times the input voltage:

$$P_{bias} = I_q \bullet V_{IN}$$

The power conduction losses are the losses of the built in transistors while fully turned on and a rough estimation is:

$$P_{cond} = \text{duty cycle} \bullet R_{dson} \bullet I_{OUT}^2$$

The switching losses are the losses that occur during the transition times of the internal transistor before and after the on time and can be estimated by:

$$P_{switch} = (I_{OUT} \bullet V_{IN})/2 \bullet F \bullet (t_{LH} + t_{HL})$$

Where F is the switching frequency and t_{LH} and t_{HL} are the transition times from low to high or high to low.

All the individual losses are sometimes difficult to calculate due to incomplete information regarding parameters such as the exact rise time, exact R_{dson} during the on time and other parasitics which are not easily characterized. Sometimes it is easier to take the over all efficiency of a given power converter board and to subtract the losses of the external components such as the external schottky diode, the inductor, current flowing through the external resistive divider, and possibly the capacitors depending on the ESR.

Once we know the losses of the switching regulator IC, the thermal analysis can be started. The individual datasheets give the thermal resistance from the junction of the IC to case (or PCB), which is referred to as θ_{JC}. The units are degrees centigrade per Watt, and knowing the ambient temperature as well as the dissipated power on the die gives the temperature of the die. The resistance value θ_{JC} has a lot to do with the package the silicon is housed in but it also includes the size of the die, the die attach material, and bond wire type and number. This is the reason why there is not one θ_{JC} per package type, and why the junction to resistance has to be thermally measured with each individual newly released IC product.

The junction to ambient thermal resistance, θ_{JA}, depends greatly on the design of the printed circuit board around the IC. Generally, datasheets give information about the PCB and layout situation in which the given thermal resistance is valid.

National Semiconductor
The Sight & Sound of Information

The precision of the analytical approach depends greatly on the complexity of the formulas as well as on the precision of data of components available to the designer. In many cases, it is more precise to use a practical approach with measurements in the lab rather than mathematical models which lack accuracy due to many unknowns.

The Simulation Approach

To simplify thermal predictions, National's WEBENCH® online simulation tool includes a module called WebTHERM® which offers thermal modeling of many switching regulator ICs, including National's new LM557x and LM2557x SIMPLE SWITCHER regulators. The thermal simulation results are given in a colorful thermal graph where hotspots can easily be detected and the temperature of each point on the board can be found. Heat sinks can be added to improve thermal dissipation. Also, airflow can be adjusted using fans from different directions. ***Figure 2*** shows a screenshot of a thermal simulation result with WebTHERM. This approach is very simple and gives a good idea of how heat dissipates across a board. It also helps to understand where hotspots exist in individual designs.

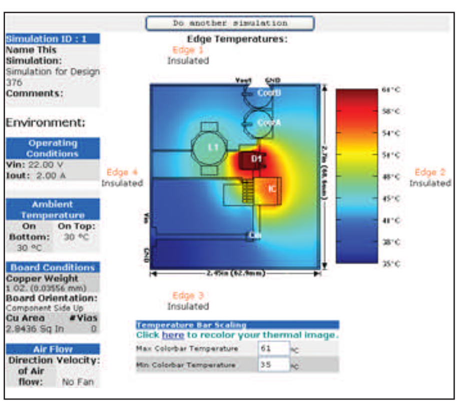

Figure 2. Thermal Simulation with WebTHERM

The Hands-On Approach

The most accurate approach in finding the true IC temperature in a design is to build the design with all the final components which will be on the board, but physically set up on a board with enough distance from component to component so that the heat dissipations of individual components do not influence the temperature of other components on the board. A clever way of achieving the same result without changing the layout is to mount components in the air on short wires. The board can then be set to run steady state and the temperature of the external components can be measured with an infrared thermometer.

In the next step, we try to heat up the external components to the exact same temperature by driving them individually. For example, we would drive the inductor with a DC current so that in steady state we would get the same infrared temperature measurement. The dissipated power needed to warm the device up to the same level as with the complete power design running can easily be calculated by multiplying the DC current by the DC voltage drop across the inductor.

Once this exercise is done for the external components, but mostly the external diode and the inductor, we can correctly measure the efficiency of the complete power design, subtract the losses of the individual external components from our measurements, and get to the power losses of the switching regulator IC.

This power loss can again be translated into die temperature using the θ_{JC} thermal resistances as given in the datasheet.

The Choice is Yours

There are many different methods for performing thermal analysis. Depending on the precision needed as well as the time and effort one is willing to put into it, there are different options as described above. If your design requires the switching regulator to work with a junction temperature up to 150°C rather than the typical 125°C maximum junction temperature, there are SIMPLE SWITCHER regulators that can help, such as National's LM2590HV-AQ. ■

For Additional Design Information

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TAKING CONTROL OF MACHINE VISION

IMPROVEMENTS IN PROCESSING POWER AND SOFTWARE AVAILABILITY ALONG WITH THE RISE IN DIGITAL CAMERAS ARE MAKING THE USE OF MACHINE-VISION SYSTEMS FOR INDUSTRIAL CONTROL AN INCREASINGLY ATTRACTIVE APPROACH. THESE TRENDS ARE SIMPLIFYING SYSTEM CREATION, BUT GETTING THE SYSTEM TO FUNCTION AS INTENDED STILL REQUIRES CAREFUL ATTENTION TO DETAILS.

BY RICHARD A QUINNELL • CONTRIBUTING TECHNICAL EDITOR

In humans, sight is one of the most important senses. Vision allows us to identify objects, examine them without touching them, determine spatial dimensions and relationships, and navigate safely through our world. The same benefits accrue to the machines equipped with vision systems, when the camera and processing are configured to match the application's needs.

Numerous applications currently employ machine-vision systems, many of them in factory automation. Vision-equipped machines inspect products for flaws, identify and sort objects, measure dimensions, and align and position materials for automated assembly. Nonfactory applications include vision-based navigation for autonomous vehicles and safety systems for automobiles. As diverse as these applications are, however, they share three common elements: a camera, a processor, and image-manipulation software.

Not surprisingly, the camera is a key element in establishing a machine-vision system's capabilities. The camera sets the level of detail, or resolution, that the system can distinguish. It also sets an upper limit on the system's frame rate, or the speed at which the system can generate images, and the shutter speed or image-capture time. Frame rate dictates how quickly the control system can obtain updates, and shutter speed affects how quickly objects can be moving through the field of view. In manufacturing systems, these factors control the manufacturing throughput that the system can handle.

Both analog and digital cameras are available for machine-vision systems. Many high-end analog cameras, however, are designed to form television images and so offer few options for either frame rate or resolution. The advent of Internet video has made available some low-cost analog cameras with other resolutions, typically VGA or fractions thereof. Such cameras may be suitable for applications that are highly cost-sensitive, but they offer limited performance. All analog cameras require the use of a separate digitizer—usually part of the frame-grabber hardware—to capture the image for processing.

Digital cameras, by their very nature, do not need external digitizers and have the additional advantage of being free from the resolution and frame rate of video standards. The explosion of digital cameras in consumer applications, from photography to cell phones, has stimulated significant advances in the technology during the last decade. Digital cameras are now available in a range of resolutions with an equally broad selection of achievable frame rates, at ever-decreasing cost. Most machine-vision-control systems use digital cameras as their "eyes."

SELECTING A CAMERA

There are a variety of trade-offs to consider in selecting a digital camera. One of the most significant is resolution versus frame rate. In general, the higher the camera's resolution, the lower the frame rate it can achieve. This trade-off stems from the way in which the image sensor of the digital camera operates.

The core of a digital camera is a CCD (charge-coupled device) that is the image sensor. As **Figure 1** illustrates, the CCD's basic configuration is a rectangular array of light-sensitive cells (picture elements, or pixels) that connect to transport cells, forming a row-and-column array. Light falling onto the array generates charges in the pixel. Command signals transfer the charges from the pixels to the transport array, where they move buck-

AT A GLANCE

- Machine vision simplifies system control based on size, shape, color, and position of objects.
- Digital cameras offer trade-offs between resolution and frame rate.
- Processor options include CPUs, DSPs, and dedicated hardware at the component level, with many board-level systems available.
- A new generation of high-performance image processors is targeting automotive applications, such as hazard-detection systems and camera systems that monitor drivers.

LIGHTING FOR MACHINE VISION

The ability of a vision system to gather accurate image information depends entirely on the light that enters the camera's lens. Inadequate or inappropriate lighting can compromise the system's ability to distinguish the details it needs for successful inspection, recognition, or measurement of the object being viewed. Although image-processing software can compensate somewhat for such factors as underexposure and overexposure, glare, reflections, and shadows can wreak havoc with many vision applications. And, if color is an important factor, the right lighting is essential for the accurate detection of color differences.

Whether you are using monochrome or color images, one important lighting parameter to consider is the stability of the illumination levels. These levels affect the brightness and contrast of the image and contribute to high signal-to-noise levels in the image. Often, ensuring illumination stability requires control over the environment. For example, some fluorescent lights change intensity 5 to 10% when the ambient temperature shifts as little as 10%. Design of a machine-vision system should seek to control illumination levels if possible and adapt to changes when control is not an option.

Artificial-illumination sources that depend on ac electricity will inevitably flicker. One way to avoid the problems that this flickering can cause is to ensure that the ac frequency is higher than the machine-vision system's frame rate, so that the exposure time of any given image integrates several cycles of light variation. Too low an ac-line frequency lowers the throughput of such systems as automated inspection stations on an assembly line.

Geometry is another important lighting factor to consider. Geometry describes the alignment between the light source, the object being viewed, and the camera. The optimum geometry depends on the object's physical characteristics, which affect the reflection, transmission, scattering, absorption, and emission of light. Different surface textures, for instance, require different lighting.

THE RIGHT GEOMETRY

Figure A, which shows the results of two light positions on the image of a glossy surface with grayscale markings, highlights the importance of lighting geometry.

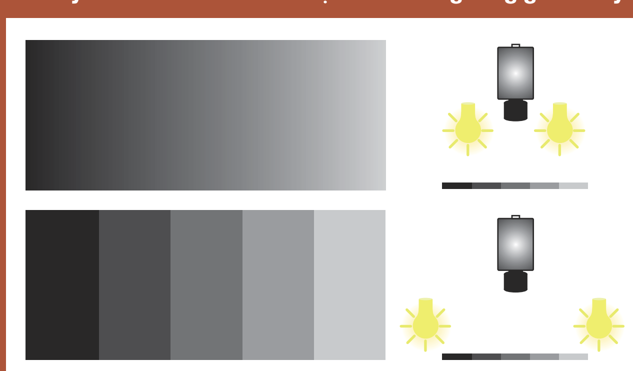

Figure A Incorrect lighting in a machine-vision system can eliminate the visibility of the features upon which the system bases control (courtesy Edmund Optics).

An illumination source high above the surface can generate glare that compromises the image, washing out differences in the markings. Placing the source at a low angle to the surface and adding a diffuser to reduce specular reflections help in the detection of small visual differences on such surfaces.

Deeply textured products, on the other hand, produce significant shadowing when the illumination source is low to the surface. If the application is examining the texture, this approach may be appropriate. If the purpose is to look for marking on the surface, however, the shadows become, in effect, visual noise for the detection algorithms.

Other surfaces may require different approaches, so knowing the object's surface qualities is essential to the creation of appropriate illumination in a machine-vision system. Fortunately, guidelines are available. The CIE (International Commission on Illumination) provides recommended lighting geometries for a variety of surfaces through its Web site, www.cie.co.at/cie.

RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Observing Maximum Ratings or How to Avoid Forecasts of Doom.

Q. How much safety margin is there in "absolute maximum" ratings?

A. None! And integrated circuits (ICs) are not fortune tellers.

An IC's absolute maximum rating is the limit of the conditions under which it may be operated. Operation beyond these limits will damage it, and may destroy it.

How far beyond the limits is never stated. Some devices are very robust, some are not, but no manufacturer will provide support for deviation from the limits. The only safe rule is to treat "never" as never. But understanding why exceeding absolute maximum limits can cause damage allows us to design better systems.

A zener diode is designed to conduct with a reverse voltage larger than its breakdown voltage and can safely carry large reverse currents. But other IC diodes, especially base-emitter junctions, are damaged by very small reverse currents, sometimes within a few microseconds. Similarly, the gate oxide of a MOS device broken down by an over-voltage is irreparably damaged. So, exceeding absolute maximum voltages may damage ICs by breaking down a junction or gate oxide.

Some absolute maximum voltages are expressed in terms of other voltages. In other words, the input voltage (V_{IN}) of an amplifier may be limited to V_{SS}–0.3 V ≤ V_{IN} ≤ V_{DD}+0.3 V, or the negative supply limit may be defined in terms of the positive supply –V_{SS} ≤ V_{DD}. The first means that the input voltage may not go more than 300 mV outside the supplies, while the second means that the magnitude of the negative supply must never exceed that of the positive supply. This does not mean that if you will be using a +10 V V_{DD} the input may go to +8

V, or the V_{SS} to –8 V *before* V_{DD} is turned on. Although silicon chips are crystals, they are not crystal balls and absolutely cannot foretell the future[1]. Absolute maximum specifications of this type indicate that power and signal sequencing is important. Exceeding this type of limit may not cause device breakdown, but is likely to turn on parasitic devices in the IC substrate, which in turn can latch up, short-circuit the power supply, and destroy the device by overcurrent or overheating.

In addition to voltage limits, the absolute maximum specification may limit chip dissipation, currents at certain pins, and chip and package temperatures. Sometimes transient dissipation and current limits may be higher than steady-state ones, but it is very important to understand — and remain within—all the prescribed limits.

[1]*Asimov, A "The Endochronic Properties of Resublimated Thiotimoline" ASF March 1948 (http://en.wikipedia.org/wiki/Thiotimoline)*

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ANALOG DEVICES

et-brigade style through the array to the charge sensor that provides the digital readout. CCDs from VGA resolution to more than 10M pixels in square or rectangular arrays are available.

A basic digital camera has only one charge sensor, so reading an image out of the camera occurs one pixel at a time. This one-at-a-time action ties the camera's frame rate to its resolution. For a given CCD-process technology, there is an upper limit to the speed at which the transport array can move the pixel charges. So, the larger the array, the longer it takes to read out an entire frame.

This trade-off is not absolute. Camera CCDs with multiple charge sensors are available. They break the image into nonoverlapping blocks that you can read out in parallel, increasing the achievable frame rate. However, balancing the multiple conversions from charge to digital value so that the independent blocks will produce matching images complicates the design effort.

It is also possible to increase the frame rate of a high-resolution camera by using only a subset of the total image. Cameras that offer this feature allow the control system to specify an image area of interest for readout rather than shift out the entire array. This approach results in a smaller image at a faster frame rate.

APPLICATION TRADE-OFFS

The optimum balance between frame rate and resolution for a machine-vision system depends strongly on the application. High resolution, for instance, is necessary when looking for small defects on large objects or making precision measurements of object dimensions. High frame rates help increase system throughput in terms of objects examined per unit time or the time needed to scan a large object.

The balance of frame rate and resolution affects camera cost. Fast multiblock and area-of-interest cameras are more costly than lower speed cameras of the same resolution. Higher image resolutions mean more expensive sensors and usually need more expensive optics in the camera to achieve the proper depth of field and field of view. Along with cost considerations, you must also factor into the camera choice such requirements as illumination (see **sidebar** "Lighting for machine vision") and color (see **sidebar** "When color matters").

The choice of camera sets the upper limit on achievable performance in a machine-vision system, but it is not the

WHEN COLOR MATTERS

Color is a subjective value that depends on an object's illumination and viewing environment as well as its spectral properties. Cameras do not see color, however; they detect levels of integrated spectral information that becomes a specific color only when a human observer views it under some set of lighting conditions. To automate color-based inspection, then, a machine-vision system must model the behavior of human eyesight.

Color in machine-vision systems typically has one of two functions. One is to use color as a basis for identification or discrimination of objects, as in a color-sorting system. Color-sorting systems need only to be able to distinguish among various, often quite different, colors, so their lighting and image processing are not particularly critical. A crayon manufacturer, for instance, can use a simple color-sorting system with standard room lighting to ensure that there is only one red crayon in each box.

The other function of color in machine vision is to monitor the color itself to ensure that it meets production specifications. If a crayon manufacturer wants to guarantee that the red crayon in each color-assorted box looks identical to that same crayon in every other box, it needs a visual-color-matching system. Only color matching can determine whether two red crayons look identical.

COLOR MATCHING

Visual-color-matching systems must judge color in the same way that humans do. One way to make this judgment is to use the "golden-reference" strategy by choosing a unit that is as close to ideal as possible. The inspection system then uses relative-color analysis to measure visual-color differences between each item it examines and the golden reference.

The precision of color-matching systems depends in part on the illumination source's spectral characteristics. The light source needs to include adequate emission at every wavelength within the visible range–380 to 720 nm–to produce results that match human perception.

The system should avoid the presence of bright spectral lines in the illumination spectrum to be able to detect metamerism: two objects that look the same under one light source but different under another light source. Metamerism occurs because human visual systems can distinguish only broad ranges, not detailed wavelength information. The additional illumination at a specific wavelength that spectral lines provide can fool the eye into seeing a color that is not inherent to the object. Few cameras detect detailed spectral information, so metamerism affects most cameras in the same manner as it affects humans.

When a system uses color matching solely for pass-fail inspections, the way in which the system quantifies the color is irrelevant; any color scheme will work. If the system is to quantify mismatches for the purpose of correcting the production process, however, the choice of color-description schemes becomes important. Standard color spaces such as the RGB (red-green-blue) of conventional digital cameras provide no insight into how a person will perceive a color. Thus, the measurement of a color error in this space does not readily translate into corrective action.

HUMAN-ORIENTED COLOR

To provide color feedback that has human significance, the vision system needs to use a color space that describes colors

only determining factor. The rate at which image processing can occur also faces limits. Several factors affect this rate, including image resolution, the type of processing needed, and the image processor's performance.

PROCESSING CHOICES

Most often, the application dictates the image resolution and type of processing, leaving designers only the choice of image processor to trade off cost and performance in the system design. Complete image-processing boards and systems in VME, PCI, and other board formats are available from companies such as Cognex, Dalsa, Epix, Matrox, National Instruments, and Philips Applied Technologies. In addition, some cameras manufacturers incorporate image-processing hardware into their products, forming a "smart camera" that is user-programmable to handle many machine-vision tasks.

Some of the choices available at the component level for creating custom image-processing systems include general-purpose CPUs, DSPs, dedicated processing hardware, and specialty image pro-

TABLE 1 COMMON MACHINE-VISION ALGORITHMS

Algorithm	Description	Usage
Histogram	Counts and graphs the total number of pixels at each gray-scale level	Determine whether the exposure and contrast of an image are suitable to the application
Spatial filters	Remove noise, sharpen, smooth, and transform images	Improve image quality
Blob analysis	Detect binary large objects (blobs) to find regions of interest in an image	Locate objects, detect flaws, identify objects
Edge detection	Locate the edges of objects	Measure objects, detect objects, determine alignment
Pattern matching	Locate regions of an image that match a template	Locate and identify objects for alignment, inspection, and measurement
Color matching	Compare the color of a region with a color template	Identification, sorting, color inspection

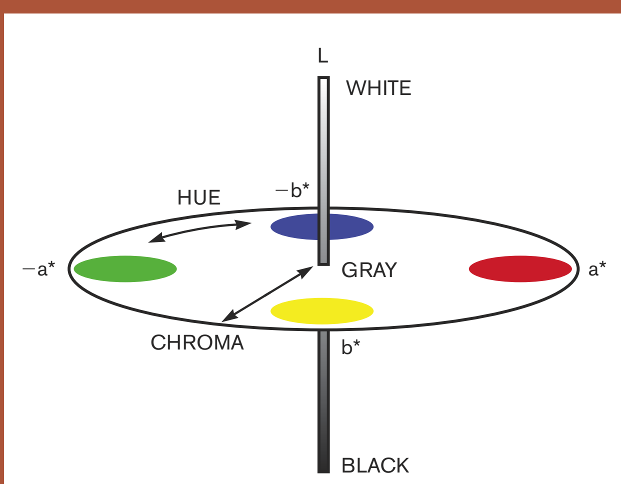

Figure A Vision systems that must measure colors and provide corrective feedback need to use a color space such as the CIE L-a-b, which describes color in human-perception terms (courtesy Edmund Optics).

in a manner similar to human perception. The CIE (International Commission on Illumination) L-a-b color standard is one such color space (Figure A). This standard uses "opponent theory," which relies on the fact that, in human perception, an object can look neither red and green at the same time nor yellow and blue at the same time.

The CIE L-a-b system uses three values–Lightness (L), a*, and b*–to quantify a color. The first, L, quantifies perceived brightness (gray level). The second, a*, represents how red or green the object looks. Positive a* values represent reddish colors, and negative values indicate greenish ones. The third parameter, b*, indicates yellowish versus bluish colors. Positive b* indicates yellow, and negative b* indicates blue.

The CIE L-a-b color space is perceptually uniform; that is, equal differences in the color space represent equal human-perceived color differences. This representation simplifies the correction of color errors. If a measurement shows that a color looks too bluish, fixing the problem becomes simple.

A similar color space is the HCL (hue/chroma/lightness) standard. Hue describes how red, green, blue, or yellow the color appears. Chroma represents the color's departure from gray, which humans perceive as saturation or vividness. Lightness describes how dark or light an object is. The lightness scale runs from black to white with gray in the middle.

These two color standards map onto one another with CIE L-a-b values translating uniquely to the HCL color space. You can calculate hue and chroma from a* and b* values. Lightness is the same in either scale. Thus, a system that can work in one representation can work in both, providing information that will help evaluate and correct color errors.

The RGB color space also maps into the human-oriented color spaces but not completely. The mapping function to cover the entire color space describable by HCL or L-a-b requires negative values for red and green in some areas. Because cameras can provide only positive output values, working in the RGB space results in an inability to describe some colors. Applications that must handle the entire color spectrum require sensors such as spectrometers or colorimeters to make color measurements.

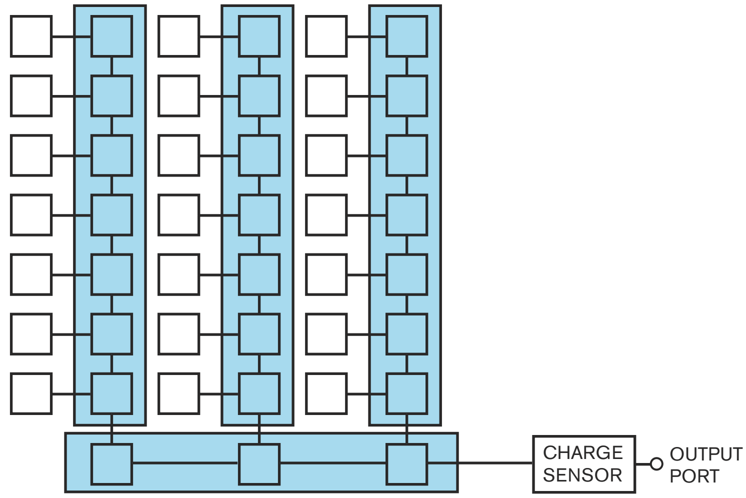

Figure 1 The image sensor in digital cameras is a CCD (charge-coupled device) that typically shifts out image data one pixel at a time, coupling image resolution with the maximum frame rate achievable (courtesy Imperx).

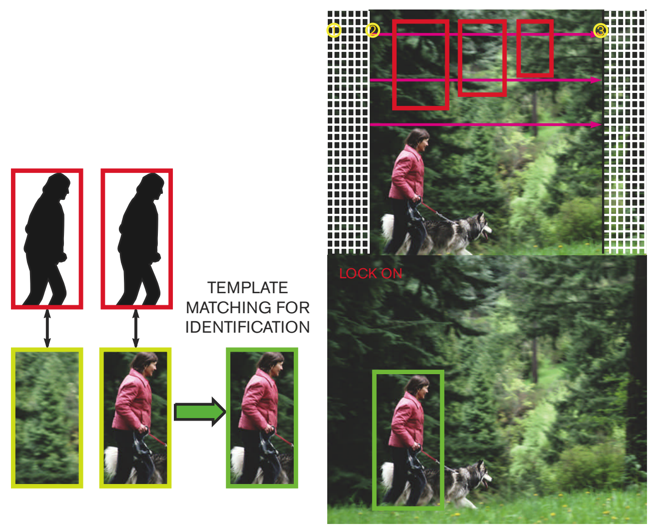

Figure 2 The latest wave of machine-vision-control systems is appearing in automobiles, identifying objects such as nearby pedestrians to warn drivers of impending hazards (courtesy NEC).

cessors. General-purpose CPUs, including PCs, are most useful if the CPU is also slated for use in other system-control tasks and if the image-processing tasks are modest, with simple algorithms and relatively low resolution and low frame rate. Dedicated processing hardware—possibly implemented in an ASIC or an FPGA—is most effective at the other performance extreme: high resolution and high frame rate. The more complex the processing algorithm, however, the more difficult the hardware design.

For the highest performance with complex processing algorithms, a software-driven DSP or specialty image processor may prove more cost-effective than dedicated hardware. A number of high-performance DSPs suitable for machine-vision applications are available from companies such as Analog Devices and Texas Instruments. These devices are well-established product lines with substantial development-tool and library support for machine-vision applications.

The specialty image processors represent a new breed of devices targeting the automotive market, although they are also useful for other vision-control applications. The automotive market for machine vision is growing, according to a

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recent report (**Reference 1**). Among the automotive applications for machine-vision-control systems are those targeting automated parking and driver safety.

Automotive-safety applications use machine vision to supplement a driver's awareness of such things as lane markings, pedestrians, and other objects in the road by identifying and highlighting them in a video display (**Figure 2**). The vision systems may also monitor the driver, looking for indications of dozing, distraction, or inattentiveness. Currently, such systems provide warnings or alerts to the driver, such as by sounding an alarm or vibrating the steering wheel, rather than take control of the vehicle. Future uses may, however, also include automatic activation of braking systems or even evasive action.

The vision task for these systems is to scan images of the road or driver to locate, identify, and assess potential hazards. This task can be as simple as locating lane markings to determine whether the driver is drifting across the road or as complex as determining the presence of a pedestrian near the vehicle, measuring the relative positions and movements of the car and pedestrian, and determining whether a collision is imminent.

AUTOMOTIVE VISION

Because these specialty processors are handling safety-critical functions, they must operate in real time using complex algorithms to help minimize false alarms. Thus, they represent some of the most powerful programmable image processors available. One product in this category is the MobilEye EyeQ image processor, manufactured by STMicroelectronics. The EyeQ uses two ARM RISC-processor cores and four proprietary VCEs (Vision Computing Engines) operating in parallel to provide high-performance scene recognition and interpretation in a single-chip device.

NEC Electronics has also announced a specialty image processor for automotive-machine-vision applications, the Imapcar for image recognition. This device uses 128 processing elements in parallel, using an SIMD (single-instruction-multiple-data) architecture to handle multiple parts of an image simultaneously. The company claims an equivalent processing power of 100G operations/sec with a 100-MHz clock.

Whether an application requires such processing power depends on the complexity of the image-processing algorithms as well as the image resolution and frame rate required. In addition, the efficiency of the algorithm's software implementation is a significant factor. Fortunately, libraries of common image-processing functions that are highly optimized for performance are widely available, both from processor manufacturers and independent software providers. **Table 1** lists a number of important image-processing functions available in software along with their uses in machine-vision-control systems.

The availability of such software along with high-performance digital cameras and ever-increasing processing power has shifted machine vision away from being a specialty requiring high levels of technical skill and programming expertise. Machine-vision systems are becoming accessible to a wider variety of control applications, in which shape, size, color, and position of objects are the key factors determining how the system needs to react. EDN

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AUTHOR'S BIOGRAPHY

Contributing Technical Editor Richard A Quinnell has been covering technology for more than 15 years after an equally long career as an embedded-system-design engineer.

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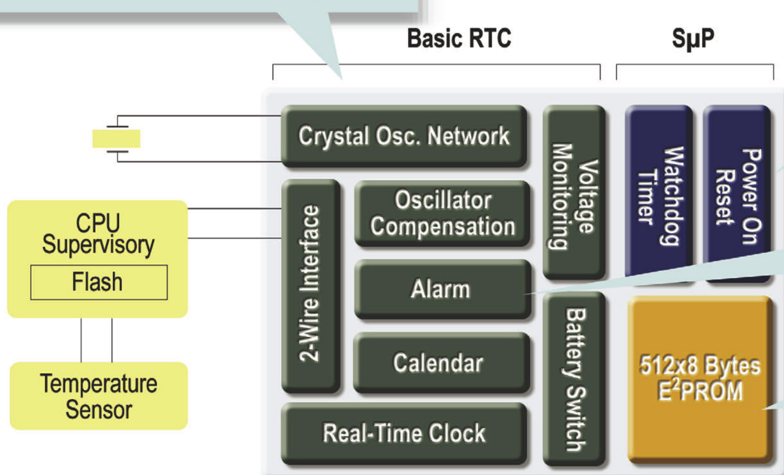

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ISL12027	512 X 8	2	Y	Y	$\overline{RESET}$		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12028	512 X 8	2	Y	Y	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP
ISL12029	512 X 8	2	Y	Y	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP

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FLANKED ON EITHER SIDE OF THE PERFORMANCE, PRICE, AND POWER CURVE BY 8- AND 32-BIT PROCESSORS, CAN 16-BIT PROCESSORS SURVIVE?

PUTTING THE SQUEEZE ON 16-BIT PROCESSORS

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

The start of the much-anticipated death of 16-bit processors is upon us. Because of insufficient forecasted demand, March 30, 2007, is the final date that Intel will accept orders for its MCS51, MCS251, MCS96, 80X18X, 80X38X, 80X486DXX, and i960 microprocessors; Intel will ship the last of these devices by Sept 28, 2007 (**Reference 1**). It is only a matter of time before the other semiconductor companies producing 16-bit processors follow. Or is it? Are 16-bit processors destined to become a footnote in the history books?

The much-heralded death of the 8-bit processor has failed to materialize, and it seems that almost everyone has acknowledged that 8-bit processors will continue to enjoy a robust place in the market. The market for 8-bit processors has not stagnated, but, rather, it continues to find new life as the smallest package, lowest power consumption, or lowest cost devices find their way into applications that were just a few years ago not economically or technically feasible. Two 2006 surveys queried embedded-system designers about their choice of processors. Even though the percentages and distribution of processor choice differ between each survey, each one showed growth in the number of respondents saying that they were using 8- and 16-bit processors in their designs (**references 2** and **3**).

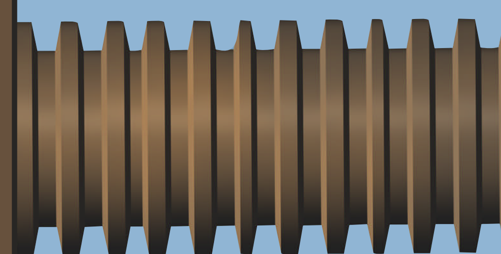
As much as high-end 8-bit processors are adding capabilities and features that compete with low-end 16-bit processors, it is the falling edge of low-end 32-bit processors reaching down into the 16-bit price range that some people have identified as the largest threat to the long-term viability of 16-bit architectures. Tensilica's Strategic Marketing Manager Steve Leibson made just such a case last year (**Reference 4**). The main point of the case is that the cost differential between 16- and 32-bit architectures continues to shrink as part of the total system cost. The point of the case continues by pointing out that there is no feature that a 16-bit architecture can implement that a 32-bit architecture cannot also implement eventually, at a nearly zero system or silicon cost differential. This fact is the crux of countless presentations from companies pitching their 32-bit architectures—companies that do not offer 16-bit products.

The 2006 update of the *EDN* Microprocessor Directory (www.edn.com/microdirectory) lists 14 companies other than Intel that offer 16-bit microprocessors or microcontrollers to the public engineering community. *EDN*'s DSP Directory (www.edn.com/dspdirectory) also includes many 16-bit DSPs. Although some of the companies with 16-bit products have not recently been publicly active with their 16-bit-product lines, many companies are continuing to invest in their 16-bit-product portfolios and are continuing to introduce 16-bit-product lines. Are these companies blindly betting millions of dollars to squeeze a little more out of a dying product line? Just what does the future hold for 16-bit processors?

At first glance, 8- and 32-bit processor architectures are squeezing out 16-bit architectures. The last few years have seen a resurgence of development effort by 8-bit-processor vendors. A previous article about 8- and 32-bit products explored why 8-bit processors best cover the low end of embedded applications in price, power, and package size (**Reference 5**). That article focuses on why 8-bit processors can fend off increasingly lower cost 32-bit devices. This article expands on the processing sweet spots that last year's processing-options article proposed (**Reference 6**).

THE SQUEEZE

Will 8- and 32-bit processors do an adequate job of overlapping and completely covering the applications that 16-bit processors best serve? To enable their 8-bit architectures to continue to support expanding requirements in leg-



AT A GLANCE

- More embedded-system designs continue to include 8- and 16-bit processors.
- Some semiconductor companies are making serious efforts to supplant the 16-bit-processor market with lower end 32-bit devices.
- Just as 8- and 32-bit architectures are evolving, so too are 16-bit devices to remain competitive.
- Lower cost and power consumption will continue to be differentiators between 16- and 32-bit processors.
- A 16-bit sweet spot is any application that couples power consumption with data-intensive processing or peripheral-task-intensive control.
- Portable or distributed monitoring and control applications are emerging opportunities for 16-bit architectures.

acy 8-bit designs, 8-bit-processor manufacturers have been expanding the capabilities and features of their 8-bit architectures. Notable expansions are a larger addressable-memory map and higher clock rates. Although these devices may be able to emulate 16-bit data types, they do so at a performance and power penalty because they must perform multiple chained operations on the low and then the high byte of the operands that 16-bit architectures would otherwise implement as single instructions. A 16-bit processor operates faster and often at lower power than an 8-bit device for applications with processor-intensive 16-bit mathematical tasks.

This performance and power penalty to process wider data types is a driver for migrating from 8-bit to wider 16- or 32-bit architectures. This point is a key transition enabling 32-bit processors to compete with 16-bit processors; it is also central to the claim that 16-bit devices are doomed. If a design team must port its design to a new architecture, why not port it to one that has much less risk of requiring another port in the near future? In this case, weighing the size of the risk and the cost of performing another port becomes a trade-off in deciding whether to use an optimized 16-bit implementation or to skip to an adequate 32-bit implementation with room to grow. For designers using soft cores in FPGAs, the choices are limited (see **sidebar** "FPGAs' 16-bit options").

In addition to more complex control functions, other drivers pushing 8-bit legacy design to consider porting to larger architectures include added functions, especially network connectivity; the need to drive larger displays; and the desire or need to use an RTOS (real-time operating system) for task management. TCP/IP (Transfer Control Protocol/Internet Protocol) network stacks require a hefty memory footprint, and there are few sources of TCP/IP stacks for 8- and 16-bit architectures. CMX Systems supports TCP/IP networking on 8- and 16-bit systems, but to support the smallest footprints, the stacks omit some protocol support. There is stronger RTOS support for 32-bit architectures than for 16-bit ones, mainly because systems implemented on 32-bit devices tend to be more complex and better benefit from RTOS support.

Last year, Luminary Micro introduced ARM Cortex-M3-based 32-bit processors at prices as low as $1. This price places the processors squarely in competition with many 8- and 16-bit processors. In addition to Luminary Micro, Atmel and NXP offer low-cost ARM7-based processors that include features to ease the port effort from 8-bit designs. Some of these features, which are uncommon in 32-bit offerings, include bitwise manipulation, brownout detection, and power-on reset. The inclusion of these "8-bit" features in these devices plays to the point of 16-bit doomsayers that 32-bit devices can outplay the 16-bit architectures.

Instruction size is another example of 32-bit architectures' ability to play along

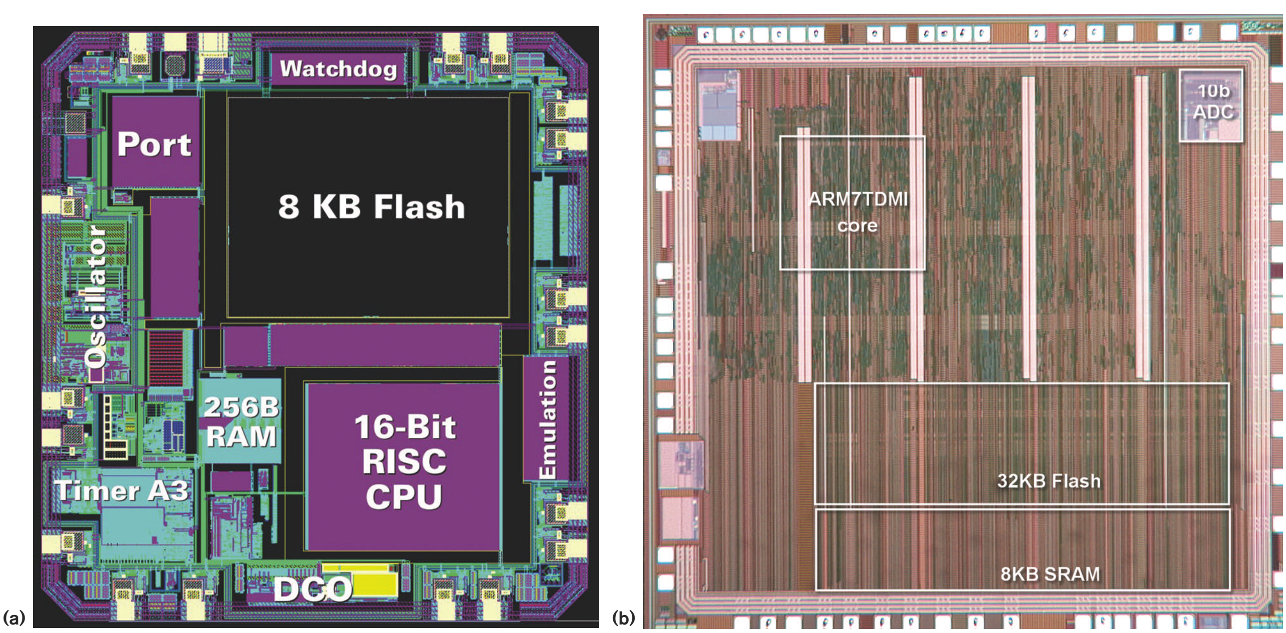


Figure 1 These die shots of a 16-bit (a, courtesy Texas Instruments) and a 32-bit (b, courtesy NXP) processor illustrate the relative silicon area of the processor core and on-chip memory (not to scale with each other).

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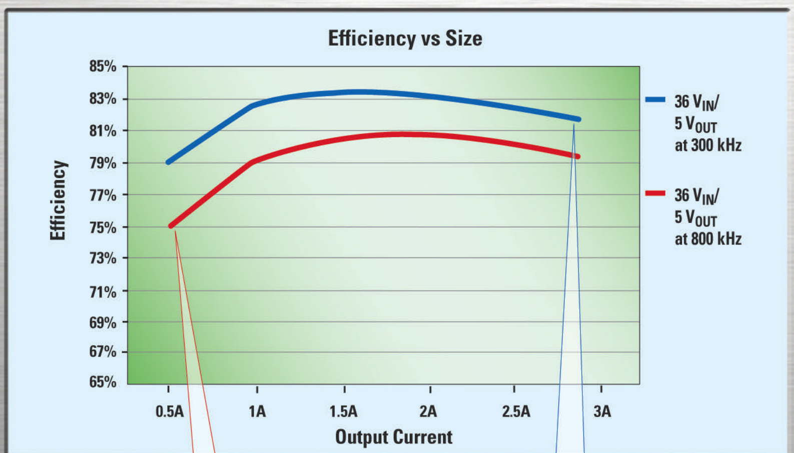

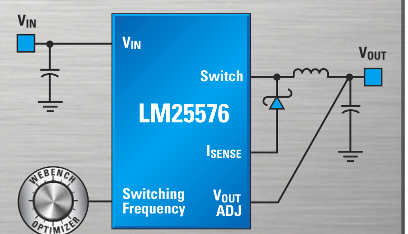

Product ID	Eval Board ID	V_{IN} Range (V)	V_{OUT} (V) Min	I_{OUT} (A)	f_{SWITCH} Range	Packaging
LM5576	LM5576EVAL	6 to 75	1.225	3	50 kHz to 500 kHz	TSSOP20-EP
LM25576	LM25576EVAL	6 to 42	1.225	3	50 kHz to 1 MHz	TSSOP20-EP
LM5575	LM5575EVAL	6 to 75	1.225	1.5	50 kHz to 500 kHz	TSSOP16-EP
LM25575	LM25575EVAL	6 to 42	1.225	1.5	50 kHz to 1 MHz	TSSOP16-EP
LM5574	LM5574EVAL	6 to 75	1.225	0.5	50 kHz to 500 kHz	TSSOP-16
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with the advantages of 16-bit architectures. In general, 16-bit ISAs (instruction-set architectures) provide significantly better code density than purely 32-bit ISAs, and this feature manifests itself in a design as smaller requirements for program memory. The impact of the advantage becomes apparent when you compare the silicon area of any 8-, 16-, or 32-bit-processor core and the memory in many systems today (**Figure 1**). This advantage is pronounced enough that many contemporary 32-bit ISAs include a 16-bit instruction subset. The Cortex-M3 ISA goes a step further, supporting only the 16-bit Thumb-2 ISA. The inclusion of a 16-bit instruction subset in 32-bit architectures substantially reduces the code-density advantage that 16-bit devices enjoyed.

THEM'S FIGHTIN' WORDS

Just as 8- and 32-bit architectures are including features that let them better compete in the 16-bit-application area, so too have 16-bit architectures been changing. For example, some modern 16-bit processors, such as Freescale's MC9S12XE 16-bit microcontrollers, break the traditional 64-kbyte address-space limitation with support for a 1-Mbyte or more linear addressing space with no paging. The memory-to-memory addressing and 16 single-cycle, 16-bit registers in Texas Instruments' MSP430 family are examples of a modern 16-bit architecture's addressing the accumulator bottleneck and limited register space in older 16-bit implementations. The 16- and 8-bit processors are including embedded debugging circuitry to assist developers.

RTOS support can help simplify programming and the process of migrating from 8- to 16-bit microcontrollers. The options have been growing for those 16-bit designs that can benefit from an RTOS. RTOS support for 16-bit architectures has lagged behind that for 32-bit architectures, but it is happening. In addition to processor-vendor-provided kernel support, RTOSs supporting 16-bit architectures are available from third-party sources, such as CMX, Mentor Graphics (Nucleus), Micrium (µC/OS-II), and FreeRTOS. To better support 16-bit RTOSs, these processors may include special on-chip registers, such as Fujitsu's User and System stack pointers, to provide additional RTOS support.

Memory protection is an important part of many embedded RTOSs, but 16-bit processors typically address system protection differently from 32-bit processors with an MPU (memory-protection unit). One example is Microchip's CodeGuard security that enables OEMs to divide and share three segments of on-chip memory with tiered levels of security for the boot, secure, and general segments. This segmentation allows design houses or algorithm vendors to protect proprietary software in secure memory segments and permit a range of applications to access the algorithm from the other segments. Other examples of some system-protection or fail-safe features in 16-bit architectures are mechanisms to protect against accidental writes to flash program memory, traps for stack overflows, an independent clock source for watchdog timers, backup oscillators, and power brownout and power-on-reset supervisors. However, MPUs are not limited to 32-bit processors; Freescale's MC9S12XE 16-bit microcontroller family includes an integrated MPU.

Despite Intel's exit from the 16-bit-embedded-processor market, more than a dozen semiconductor companies still have active 16-bit-product lines. Many of them have processor-product lines that span 8-, 16-, and 32-bit architectures. Wayne Chavez, Freescale's automotive-product-marketing manager, points out, "16-bit processors are still a source of growth, and Freescale's processor strategy is one of intelligent overlap." Many of the semiconductor companies that have processor products that span all of the data widths share this sentiment. In general, these companies place a lot of value on providing designers the ability to scale up and down for the best price, performance, and peripheral mix by preserving the programming model and tools across processor architectures. Ultimately, the main concern is that one of their processors gets the design-in, and providing a scalable choice is part of their strategy to accomplish this goal.

Another concept, virtualization, is undergoing a resurgence from the old mainframe days. At a basic level, it means allowing the software-development model to not worry about whether it resides on a single processor or on multiple cores. It can enable a hard RTOS to operate with a general-purpose operating system on the same device. However, "Most embedded-software development still relies on an intimacy with the metal for best cost and efficiency," says Ryan Scott, marketing manager for industrial and multimarket microcontrollers at Infineon. Predictable or deterministic performance, lower power consumption, and a BOM (bill-of-materials) cost difference of

FPGAs' 16-bit options

Most FPGA companies offer and support 8- and 32-bit soft cores, but none currently support a 16-bit core. Mike Thompson, senior IP (intellectual-property)-product-marketing manager at Actel, says that the company periodically receives requests to support a 16-bit core but notes, "There is not enough traction to justify the additional cost to add and maintain a third architecture." Bob Garrett, senior marketing manager for Nios marketing at Altera, acknowledges that the company's Nios 1.0 core was originally a 16-bit core but that the currently supported configurations of the core are 32 bits.

As a side note, FPGAs implemented alongside 8- or 16-bit processors in general act as external logic, a high-speed state machine, or a bridge for emerging niche functions. Power consumption is a significant challenge facing FPGAs in applications using these smaller processor architectures. According to Ritesh Tyagi, director of marketing for the System LSI Business Unit at Renesas Technology America, states, "As microcontrollers integrate hard-block implementations of these emerging functions, the new microcontrollers are replacing the FPGA."

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even a penny still matters for embedded-system designs that 8- and 16-bit processors best suit.

ESCAPING THE SQUEEZE

Low cost and low power consumption are important differentiators for 8-bit processors. Unsurprisingly, the same situation is true for 16-bit processors, especially when design teams perform a trade-off to migrate their design between 16- and 32-bit options. Designs that target 16-bit processors in general use less memory than those designs that would target a 32-bit processor. Despite the diminishing silicon differential between a 16- and a 32-bit core relative to the entire system, the appropriate amount of adjacent memory for each core size limits how close the price of these devices can converge.

In many embedded-system applications, especially those suited to a smaller architecture width, there is often a significant opportunity for lower power consumption through low-power sleep and standby modes. However, increasing leakage current—the power consumption when the processor is on but idle—negates the advantages that smaller process geometries provide in silicon area for converging the cost between 16- and 32-bit processors. Clever clock gating does not get around the leakage-current penalty. The only way to avoid it is to use slower, less leaky transistors or to be able to completely shut down and provide power to the circuit on a demand basis, further increasing the complexity and cost of the 32-bit device. Just as with performing 16-bit arithmetic with an 8-bit processor, a mismatch of data size and processor width can adversely affect the amount of overall processing the core can perform and the amount of power it takes to perform those tasks when compared with an architecture width that matches the data width.

There is no 8051 or ARM equivalent for the 16-bit-processor market. This fact may play heavily in the assumptions foretelling the death of 16-bit architectures; however, this issue may not be significant because 16-bit devices should be able to stave off 32-bit processors and defend their existence with configurations that are highly tuned for specific applications. The question, then, could be: What are those applications? Currently, automotive and industrial-control applications are major market segments for current 16-bit processors.

A processing sweet spot for 16-bit devices is any application that couples sensitivity with power consumption and data-intensive processing or peripheral-task-intensive control that 8-bit products cannot as efficiently provide. Such applications include metering for electricity, water, and gas, as well as handheld products, such as small point-of-sale products for taking orders in restaurants, retail stores, or service establishments.

In recent years, a number of semiconductor companies have built hybrid processors, which the industry increasingly refers to as DSCs (digital-signal controllers). These devices combine characteristics of DSPs and microcontrollers in a single instruction stream. Generally, DSCs can continuously feed the arithmetic unit without stalling, and they can perform rapid context switching for peripheral-control functions. These devices also commonly employ intelligent or autonomous peripheral capabilities to avoid starving the arithmetic engine. Most of these devices employ a 16-bit architecture.

Emerging applications that 16-bit architectures and DSCs are well-positioned to support include portable, home-based medical equipment; portable monitoring equipment; and distributed industrial-monitoring and -control equipment, such as for smart buildings. Most of these applications will also support wireless- or wired-network connectivity. Only time will tell whether the 16-bit doomsayers will relent as the 8-bit doomsayers have done in recent years. **EDN**

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A deep dive into HD for video-system design

THE DIGITAL-VIDEO REVOLUTION IS NOW WELL UNDER WAY. IS THE TIME RIGHT FOR YOU TO SUPPORT HIGH-DEFINITION RESOLUTIONS?

Technological advancements of recent years have enabled new video capabilities in end equipment ranging from cell phones and MP3 players to video walls and billboards. Because of the strong demand and level of innovation that characterize digital-video markets, system manufacturers must consider what form of video to include in their new products. One of the major issues is whether to provide for HD (high-definition) displays, which offer much better image quality than viewers were accustomed to in the past. Given the market's forward impetus toward bigger and better equipment, the answer would seem to be a no-brainer: yes.

But it's important that video-system developers be clear about what HD involves to avoid the impression that everything must be HD. You can call a variety of display formats "high-definition," and some or all of these may be inappropriate in certain applications. In addition, you must weigh the quality of the display against the level of signal compression. And, in any system, there is an issue of cost. The real question, then, is not so much *whether* an application requires HD, but how to achieve the best possible quality given the system's display, bandwidth, and storage constraints, as well as consumers' price expectations. Once you determine this issue, you can select an underlying process-

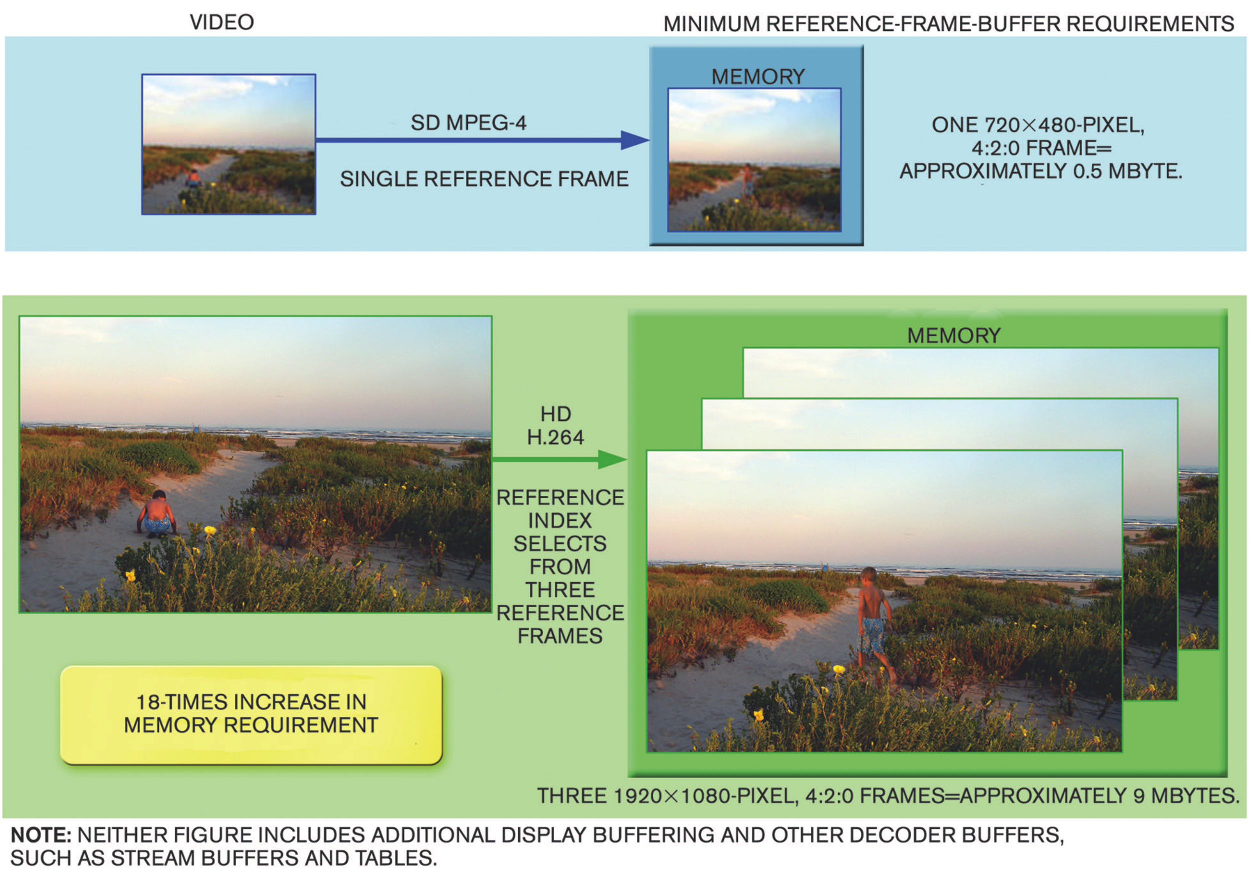

Figure 1 Decoding HD video requires significantly more memory, especially when you have employed advanced video codecs to compress it, than is necessary with SD video.

TABLE 1 COMMON DTV-DISPLAY FORMATS

	Resolution (pixels)	Aspect ratio	Refresh rates (frames or fields/sec)*	Notation examples
HDTV	1920×1080	1.78-to-1	24p, 25p, 30p, 50i, 60i	1080i60
	1280×720	1.78-to-1	24p, 25p, 30p, 50i, 60p	720p30
SDTV	720×576	1.33-to-1	24p, 25p, 50i, 50p	576i50
	720×480	1.33-to-1	24p, 30p, 60i, 60p	480i60

*Frames per second for progressive (p) scans and fields per second for interlaced (i) scans. Two interlaced fields make a frame.

ing technology that meets the general system requirements for performance, flexibility, and cost efficiency.

WHAT DOES "HIGH DEFINITION" MEAN?

Looking for an all-inclusive description of HD reveals how slippery the term can be. For most people and in most uses, "HD" refers to HDTV, with its wider screen and higher resolution than traditional SDTV (standard-definition TV). Although the width-to-height aspect ratio for SDTV is 1.33-to-1 (4-to-3), HDTV at 1.78-to-1 (16-to-9) is closer to the dimensions of most cinema releases, so there is less need for cropping or letterboxing to fit film images onto the screen. The top resolution that manufacturers define for HDTV offers six times the visual information of SD, making details appear correspondingly crisper and colors more intense. Because of the digital transmission of HDTV, pictures either come through, or they do not: The snowy, washed-out images and vertical rolling of analog broadcasts are things of the past. A digital source also enables multiple images to simultaneously fit onto the same screen for easier channel surfing or reference to programming schedules and other information. When multispeaker surround sound adds to these visual advantages, the result can be an astonishing new experience in home entertainment.

The appeal of large, brilliant screens that closely mimic the movie-theater experience is the driving force when it comes to marketing the new digital-transmission technology to consumers. But HDTV is not synonymous with DTV (digital TV), which has a broader definition, though public perception may have confused the two terms. Manufacturers have been phasing in DTV in the United States over the last several years, with the governing ATSC (Advanced Television Standards Committee) defining a number of commonly used digital-broadcast formats. DVB (Digital Video Broadcasting), the equivalent international organization, has also defined formats that overlap with the ATSC formats.

Table 1 lists some of the common display formats for DTV, showing that there are a number of HDTV formats. Almost all HD displays are now progressive-scan, and HDTV sets with 1080p (1920×1080-pixel resolution, progressive scan) have only recently become available. In countries that transmit PAL (phase-alternation-line)- or SECAM (séquentiel couleur avec mémoire)-based analog television, refresh rates of 25 and 50 frames/sec find use, rather than the NTSC (National Television System Committee) rates of 30 and 60 frames/sec in the United States. The 480i60 (720×480-pixel resolution at 60 frames/sec, interlaced-scan) SD format provides a digital approximation of NTSC analog-TV reception, whereas 576i60 is a digital approximation of PAL and SECAM. HDTV screens can also display these SD formats, though not at the full screen width. Manufacturers sometimes market the 480p60 and 576p60 formats, as well as some resolutions that standards do not list, such as 1080×720 pixels, under the label EDTV (extended-definition TV). For compatibility with film, standards define 24 frames/sec for use in video production, though it is not a broadcast-transmission rate.

WHAT ELSE MIGHT "HD" MEAN?

Digital video also has low-end resolutions, which some refer to as LDTV (low-definition TV), which often finds use in Internet streaming and low-end video. In these low-end formats, the basic unit is CIF (Common Intermediate Format), which at 352×288 pixels is roughly one-quarter of the SD-screen resolutions. CIF and its subdivisions, such as QCIF (quarter CIF, or 176×144 pixels), are familiar in computer streaming video and provide the basis for divided-screen applications on DTVs. CIF also has its multiples: 4CIF (4 times CIF, or 704×576 pixels), 9CIF (9 times CIF, or 1056×864 pixels), and 16CIF (16 times CIF, or 1408×1152 pixels). These higher end CIFs overlap in scale with but do not match the HDTV formats, so you can use LDTV to build HD formats that do not correlate with HDTV resolutions.

At the high end, new formats, such as the lab-demonstrated UHDV (ultra-high-definition video), are appearing that even further push display technology. UHDV provides 16 times the pixels of a 1920×1080-pixel image. Even without going to these spectacular lengths, you can find equipment that goes beyond HDTV resolutions in digital-cinema and commercial-

TABLE 2 PERFORMANCE REQUIREMENTS FOR REPRESENTATIVE HD APPLICATIONS

HD encode application	Key priorities	2006 technology	Memory requirements	Video bit rate	Typical display format	Typical codec
Broadcast HDTV	High quality for high-action sports	Tens of 1-GHz DSPs and FPGAs	Multiple gigabytes	10 to 20 Mbps	1080i60	MPEG-2, H.264 High Profile
Videoconferencing	Low latency, best resolution for available bandwidth	Multiple 720-MHz DSPs	Hundreds of megabytes	More than 1 Mbps	720p30	H.264 Baseline Profile
Digital still camera	Low-complexity quick printing from video	Single-chip, 450-MHz, low-power system on chip	32 to 64 Mbytes	4 to 8 Mbps	720p30	MPEG-4 (part 2) Simple Profile

video production. In addition, a range of HD-computer-graphics formats sometimes finds use in video display. Although these computer-graphics formats traditionally exhibit the 1.33-to-1 SD aspect ratio of CRTs, some of the recent variants incorporate support for wide-screen LCDs that can handle HD-digital video, among other applications. These wider formats include WXGA (wide extended graphics adapter) at 1280×800 pixels, WSXGA+ (wide super XGA+) at 1680×1050 pixels, and WUXGA (wide ultra XGA) at 1920×1200 pixels, all with aspect ratios of 1.6-to-1. Refresh rates for these formats are almost always progressive-scan and much faster than DTV rates. Although these formats differ from the HDTV-standard formats, computer- and DTV-display technology is so closely linked today that most HDTV sets actually use VESA (Video Electronics Standards Association) resolutions, such as WXGA, with the TV converting the video from the broadcast or recorded format to the actual display format.

OTHER FACTORS AFFECTING IMAGE QUALITY

Clearly, a developer had better understand the range of display requirements for a system before undertaking an HD design. Just as important as the technical requirements, though, are the perceptual ones: How an end user employs the system can make an even bigger difference than the format of the display. First, HD's effects are perceptible only with large displays: At less than 40 inches diagonally, the display largely loses the extra resolution. Obviously, HD would be pointless for a handheld display on a cell phone. But even in a small display for, say, viewing in the back seat of a car, a viewer cannot tell the difference between HD and SD.

Second, the effect of surround sound is even more dramatic than that of a high-resolution display. In other words, great sound will make a so-so image seem better, whereas inadequate sound will diminish the effect of a great image. Manufacturers should look to improve audio along with, or even before, video.

The third factor affecting image quality is video compression and decompression. Normally, the system compresses digital video to reduce the enormous bandwidth it requires, which, uncompressed, would exceed 124 Mbps for the SDTV broadcast formats and approach 750 Mbps for 1080i60. Storage also is a factor, because single-layer DVDs can hold approximately 4.7 Gbytes of data—enough for only short clips of uncompressed video. Double-layer HD DVD and Blu-ray discs extend storage to approximately 30 and 50 Gbytes, respectively, but they still require a huge amount of compression to hold hours' worth of video content.

The Main Profile of MPEG-2 (Moving Pictures Experts Group 2), the best established and most widely used standard for video compression, normally provides high-quality, source-dependent compression at ratios of approximately 30-to-1 to 50-to-1, using 4:2:0 color sampling. Because H.264, also known as MPEG-4 AVC (Advanced Video Coding) and as MPEG-4 Part 10 Main Profile, roughly doubles this level of compression, the video-broadcast and -recording industry will be moving to the new standard during the next few years. All of the ITU (International Telecommunications Union)/MPEG standards are lossy, however, so the played-back decompressed image is by nature less well-defined than the original image before compression. Because the images are in motion and because the standards' developers based them on a great deal of study about how people perceive images, the technologies conceal the loss of image definition so well that it is generally unnoticeable. However, pushing this loss beyond the approximately 60-to-1 to 100-to-1 compression ratio of H.264's High Profile risks revealing flaws in the image; these flaws show up much better with HD displays.

SYSTEM RESOURCES

Decompressed 1080i60 video requires six times the amount of data that decompressed SD video requires, and 720p60 more than 5.3 times as much. In raw terms, therefore, the system

TABLE 3 CODEC TRENDS BY APPLICATION

Application	Current algorithms	Future codec considerations
Security/surveillance	Motion JPEG, H.263 MPEG-4 Simple Profile	JPEG2000, H.264 Baseline, WMV9
Videophone/ videoconferencing	H.263, H.261	H.264 Baseline
Internet streaming	Windows Media, Real Video, DivX, MPEG-4	Frequent updates, PC platform has allowed support for proprietary codecs
DVD	MPEG-2 MP at medium level	H.264, VC-1 required for HD-DVD and Blu-ray DVD
Digitial-terrestrial TV	MPEG-2 MP at medium level, MP at high level	Opportunity for advanced codecs in regions without installed base
Satellite	MPEG-2	Moving to H.264 High Profile to boost HD-channel capacity
DSL-based video on demand	MPEG-1, low-resolution MPEG-2 with bandwidth limitations	WMV9, H.264 Main Profile, On2 VP6
Digital still cameras	Motion JPEG and MPEG-4 Simple Profile	H.264 Baseline
Digital-video camcorders	DV-25	MPEG-2, MPEG-4
Cellular media	MPEG-4 Simple Profile	Real Video, H.264 Baseline, AVS-M

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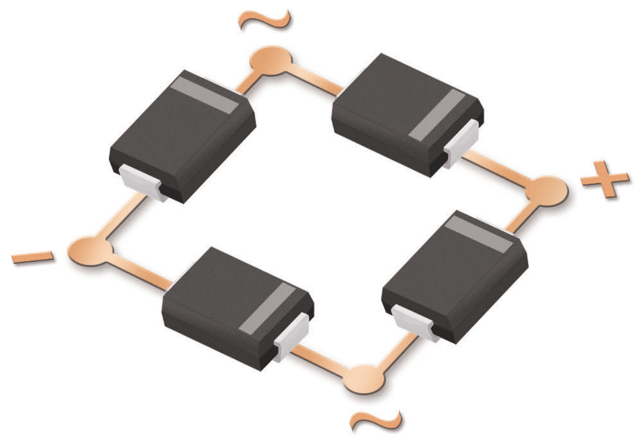

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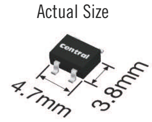

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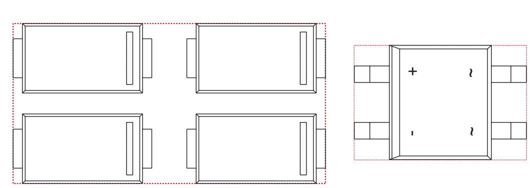

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must provide six times the processing throughput and memory for HD as it would for SD. Moreover, because the more advanced codecs achieve greater compression by employing more memory and processing, the system requirements become correspondingly higher. For instance, the memory requirement for an MPEG-4 Simple Profile 480i30 SD decoder for reference-frame data is approximately 500 kbytes, whereas the minimum requirement for an H.264 High Profile decoder for 1080i60 HD is about 9 Mbytes—18 times higher. This increase comes not only from the greater HD pixel resolution, but also from the fact that MPEG-4 Simple Profile requires only one frame for its frame-prediction algorithm whereas H.264 Level 4.0 High Profile requires five frames. For HD decoding, the processor therefore must have 18 times the available memory for internal reference-frame buffers. It also requires additional memory for display buffering and other decoder functions, such as stream buffers and tables (**Figure 1**).

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Table 2 summarizes the general system requirements of three representative and widely varying HD-codec applications. The first, broadcast HDTV, outputs the highest bit rate and operates in real time using either MPEG-2 or H.264 for compression. Using today's technology, broadcast systems that compress HDTV programs for transmission require numerous high-frequency DSPs (digital-signal processors) and FPGAs (field-programmable gate arrays), supported by several gigabytes of memory. A number of these devices, in a "blade" arrangement, may operate as a parallel-processing farm to provide multiple channels of compressed-HDTV output.

Another application, videoconferencing, needs to scale to accommodate the low-megabit-range bandwidths available through many WAN (wide-area-networking) links yet still be able to provide an HD image that can appear on a large display. Latency in the video-coding and -decoding process must be minimal to not interfere with conversation. Given the transmission requirements and assuming that you are using the H.264 Baseline Profile for compression, the 720p30 HD format—somewhat lower in resolution than the HDTV example but still high end—is practical. Today's technology requires several DSPs and hundreds of megabytes of memory to satisfy this application.

A common consumer application for video compression is in DSCs (digital still cameras), which can capture short video clips for viewing on HD displays. DSC systems have to be easy-to-use and inexpensive, both factors leading to the use of MPEG-4 Simple Profile to minimize processing and memory requirements. A single highly integrated DSP-based SOC

(system on chip) for portable-system applications can perform the codec requirements of this application (**Table 3**).

SYSTEM COST AND VERSATILITY

Obviously, the requirements of HD systems vary widely, depending on bandwidth and compression levels, as well as display formats. Video clips stored using a DSC would look primitive in a broadcast application, for example, whereas an HD-broadcast bit stream would overwhelm a videoconferencing system with data. But, at any level of application, HD formats will have considerably greater requirements for memory and processing than SD formats do. These requirements translate into higher component costs, which, like almost all semiconductor costs, will diminish predictably over time. For the system manufacturer, then, the fundamental question may be whether to build in HD support now at today's cost or stay with SD support for the next year or few years until component costs are lower and HD demand has increased.

Manufacturers must also consider the versatility of their designs, because virtually every digital-video system today has to take into account the continual introduction of, and improvement in, codecs. The influence of H.264, whether for DTV broadcasts, IPTV (Internet Protocol TV), videoconferencing, or other applications, will be significant in the next few years. Competing standards, such as WMV9 (Windows Media Version 9)/VC-1 and China's AVS (Audio Video Coding), and the ITU/MPEG standards all offer variations in implementation. Systems such as set-top boxes may have to dynamically deal with a number of standards and variations, interface with entertainment and gaming consoles, and support home-computer networks and, eventually, videophones.

It may be important for such a system to not only decode, but also transcode and transrate, video streams to support different displays and handle application and control software. Even an application such as video surveillance needs the ability to upgrade its codec and add features such as object analysis and recognition. When you add variability of video-input-stream formats and end applications to the variety of potential HD outputs, the need for system flexibility becomes apparent. Designers must bear this need in mind as they select an enabling technology for their video systems.

SELECTING A MEDIA PROCESSOR

To support the high-throughput, multiple-application requirements of an HD-video system, a processor must provide both performance and versatility at a reasonable cost. By design, DSPs supply a high level of performance for handling real-time algorithms, such as audio/video codecs and HD-rate data streams. Processors that integrate both DSP and RISC (reduced-instruction-set-computer) cores have the

additional advantage of being able to partition performance between the DSP for signal processing and the RISC for control, communications, and applications software. Multicore DSPs for audio/video applications also include VICPs (video-image coprocessors) that provide hardware acceleration for operations that video codecs frequently use; they also provide additional on-chip hardware, such as video scaling and blending of graphics and video for creating the on-screen display to further offload video-display processing.

Programmable DSPs provide the flexibility to support a variety of codec and display standards, and they also allow quick system adaptation to accommodate new functions. In addition, you can readily reprogram the same basic design to meet requirements for different market segments and regions. DSPs have in recent years also become more user-friendly by offering a comprehensive, open-software platform with audio/video APIs (application-programming interfaces) that make the DSP transparent, so that the developer has only to program the RISC using C and standard development tools. Finally, DSPs that feature SOC integration with a memory subsystem and peripherals for video can help minimize system costs even in systems with HD and other advanced video features. **EDN**

AUTHORS' BIOGRAPHIES

Jeremiah Golston is a distinguished member of the technical staff for Texas Instruments and the chief technical officer for the company's DSP video-products business. He is responsible for TI's device-architecture road map for emerging markets in IPTV and media convergence in the connected home. Golston was a lead architect for the TMS-32064x instruction set and the DaVinci media-processing SOC platform. He holds patents in media-processing architectures and algorithms. Golston earned bachelor's and master's degrees in electrical engineering from the University of Missouri—Rolla.

As Texas Instruments' DSP-business-development manager, Gene Frantz is responsible for creating businesses that use DSP technology. Frantz joined TI's consumer-products division in 1974. While in that division, he took a leadership role in the development of TI's educational products: He was the program manager for the Speak & Spell learning aid and led the development team for all of the early speech products for TI. In 1984, he transferred to the semiconductor group's DSP department to become the application manager. Frantz became TI's principal fellow in 2002. He received his bachelor's degree in electrical engineering from the University of Central Florida (Orlando) in 1971, his master's degree in electrical engineering from Southern Methodist University (Dallas) in 1977, and his master's in business administration from Texas Tech University (Lubbock) in 1982. He is a fellow of the Institute of Electrical and Electronics Engineers and holds 30 patents in the areas of memories, speech, consumer products, and DSP. His personal interests include playing in his church's orchestra and collecting baseball cards.

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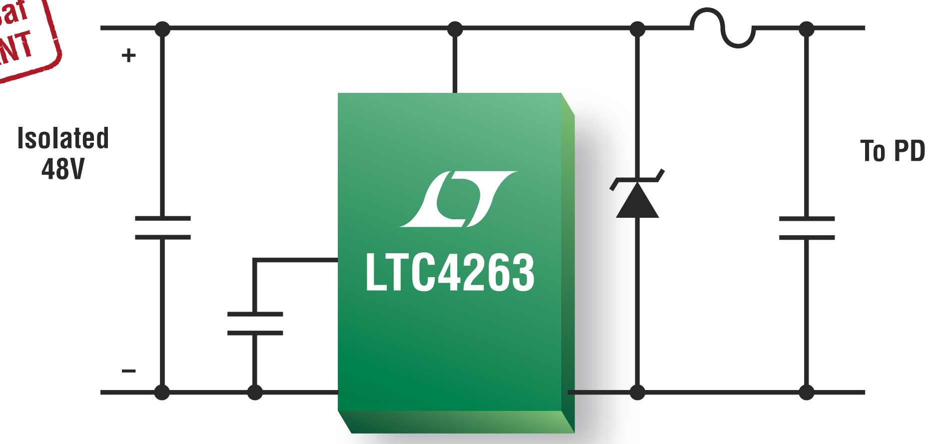

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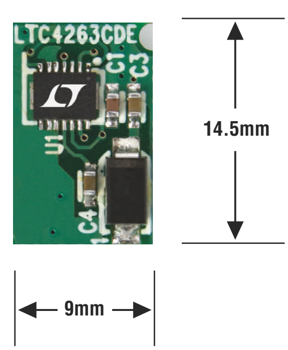

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LINEAR TECHNOLOGY

Gain-of-two instrumentation amplifier uses no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

An instrumentation amplifier offers precise gain without feedback resistors, and, at any value of gain, it provides high input impedances at its noninverting and inverting inputs. In a typical IC instrumentation amplifier, a single resistor that connects across two gain-adjustment pins determines the circuit's overall gain. Integrated versions of most instrumentation amplifiers allow the pins to remain open for unity gain but require finite-value gain-setting resistors for gains exceeding one. Although the gain-adjustment resistor might comprise a tiny surface-mounted device, its electrodes and internal resistive layer extend the conductive surface connected to the IC's gain-adjustment pins. The extended surface acts as an antenna and thus makes the amplifier more susceptible to stray external electromagnetic fields.

Figure 1 shows an instrumentation amplifier that offers a gain of two without using any external resistors. The circuit comprises a cascade of a symmetrical, differential-output amplifier, formed by two channels of IC_1; an Analog Devices (www.analog.com) AD8222 instrumentation amplifier; and a difference amplifier comprising one half of IC_2, a second AD8222. All three instrumentation-amplifier sections in the circuit provide a standalone gain of one. Because the differential outputs of the first stage have opposite signs, their difference is twice

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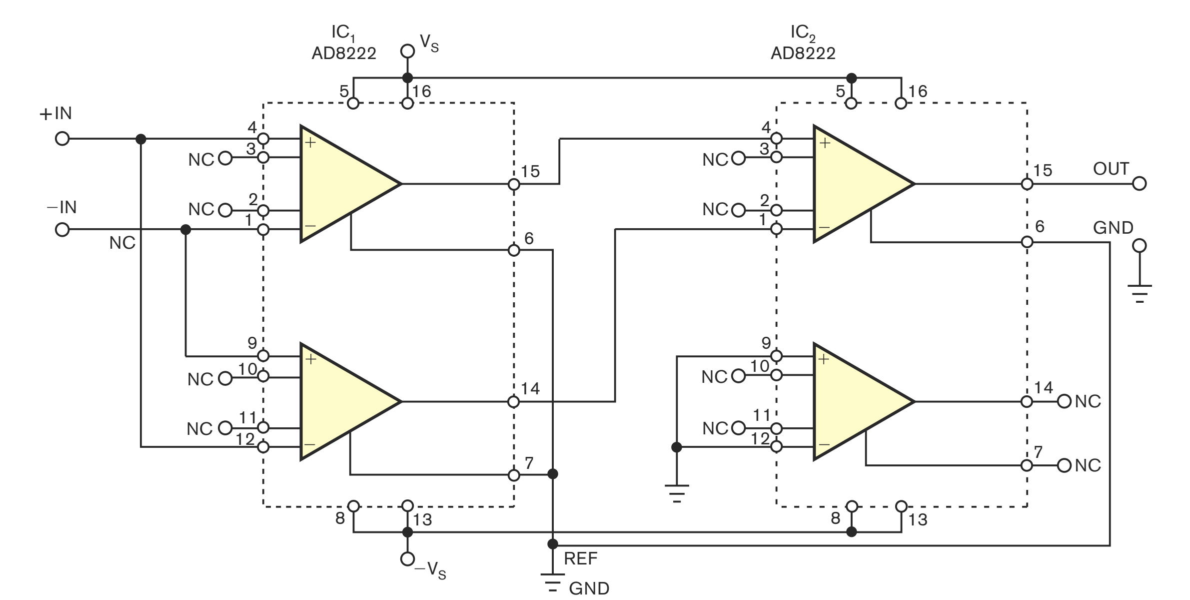

Figure 1 Based on two dual-section instrumentation amplifiers, this composite instrumentation amplifier offers a gain of two with an error margin of less than 0.06% and requires no gain-setting resistors.

that of the difference of the input signals.

The circuit's worst-case gain error does not exceed the value of $\delta_2=3\delta_1$, where, at a gain of one, δ_1 represents the maximum gain error of one section of the AD8222. For B-grade ICs, you calculate the value of δ_2 as $\delta_2\leq$ 0.06% (**Reference 1**). Typically, the value of δ_2 rarely reaches its maximum value. Given the reasonable assumptions that all three amplifiers' gain errors are independent and obey a gaussian distribution, the probability of occurrence of $\delta_2=3\delta_1$ is about 1/20 the probability of encountering a single amplifier that has a maximum gain error of δ_1.EDN

REFERENCE

1 "AD8222 Precision, Dual-Channel Instrumentation Amplifier," Analog Devices Inc, www.analog.com/en/prod/0,2877,AD8222,00.html.

Analog switch converts 555 timer into pulse-width modulator

Jordan Dimitrov, Tradeport Electronics, Vaughan, ON, Canada

This Design Idea describes a new approach to producing a variable-duty-cycle waveform from a 555-based free-running oscillator. The circuit's wide modulation range, highly linear control over a wide range of duty-cycle values, and excellent linearity make it ideal for PWM (pulse-width-modulation)-based control applications. **Figure 1** shows the basic circuit, which works as follows: When IC_1's output goes high, switch S_1 closes, and IC_1's internal discharge, switch S_2, opens. Capacitor C_1 charges through R_1 and R_2. When IC_1's output goes low, S_1 opens, and S_2 closes, discharging C_1 through R_2 and R_3.

The generic configuration works well for producing a fixed-value duty cycle.

(continued on pg 86)

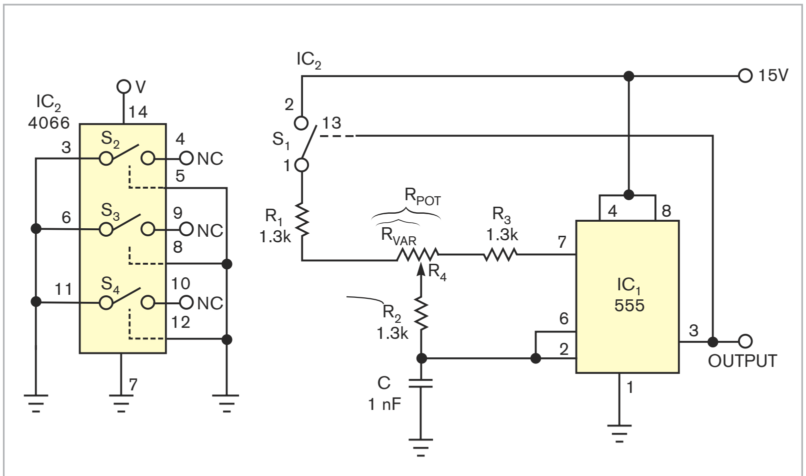

Figure 2 Add a potentiometer, R_4, to produce an output pulse that has a manually variable duty cycle.

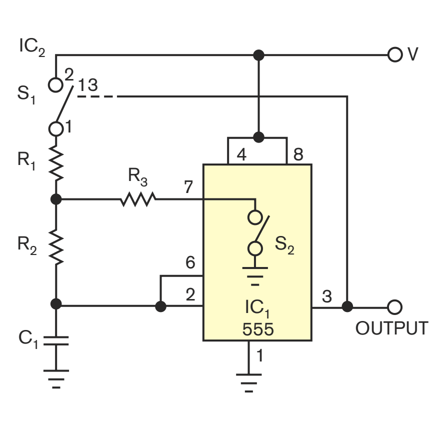

Figure 1 An external analog switch and a 555 timer provide a free-running oscillator with a fixed duty cycle.

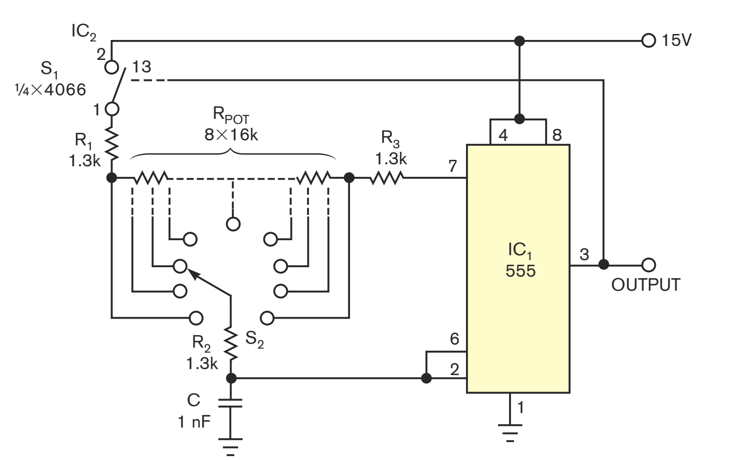

Figure 3 To obtain fixed-duty-cycle values for linearity evaluation, you can replace the potentiometer with a rotary switch and a series-connected string of precision resistors.

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LINEAR TECHNOLOGY DESIGN NOTES

Triple Output 3-Phase Controller Saves Space and Improves Performance in High Density Power Converters

Design Note 409

Mike Shriver

Today's telecommunications, server and network applications require power from a multitude of voltage rails. Having more than ten rails ranging from 5V to 1V or less is common. These boards are typically crowded with heat-producing FPGAs or microprocessors, thus demanding power converters that are both compact and highly efficient. Furthermore, the converters may need to meet other requirements such as a fast load step response and rail tracking.

The LTC®3773 switching regulator meets and even goes beyond the above requirements. This device is a 3-phase, triple output synchronous buck controller with built-in gate drivers packaged in either a 5mm × 7mm QFN or a 36-pin SSOP. Its switching frequency can be set to 220kHz, 400kHz or 560kHz, or it can be synchronized to an external clock between 160kHz and 700kHz. The controller can step down from input voltages as high as 36V and the output voltage can be programmed from 0.6V to 5V.

Figure 1 shows a high density triple output DC/DC converter with each output delivering up to 5A using the LTC3773 controller. Figure 2 shows the efficiency of each output versus load current; where up to 93% efficiency is achieved. Reductions in space are realized by the use of dual channel FETs and a switching frequency of 400kHz which permits the use of 7mm × 7mm ferrite inductors.

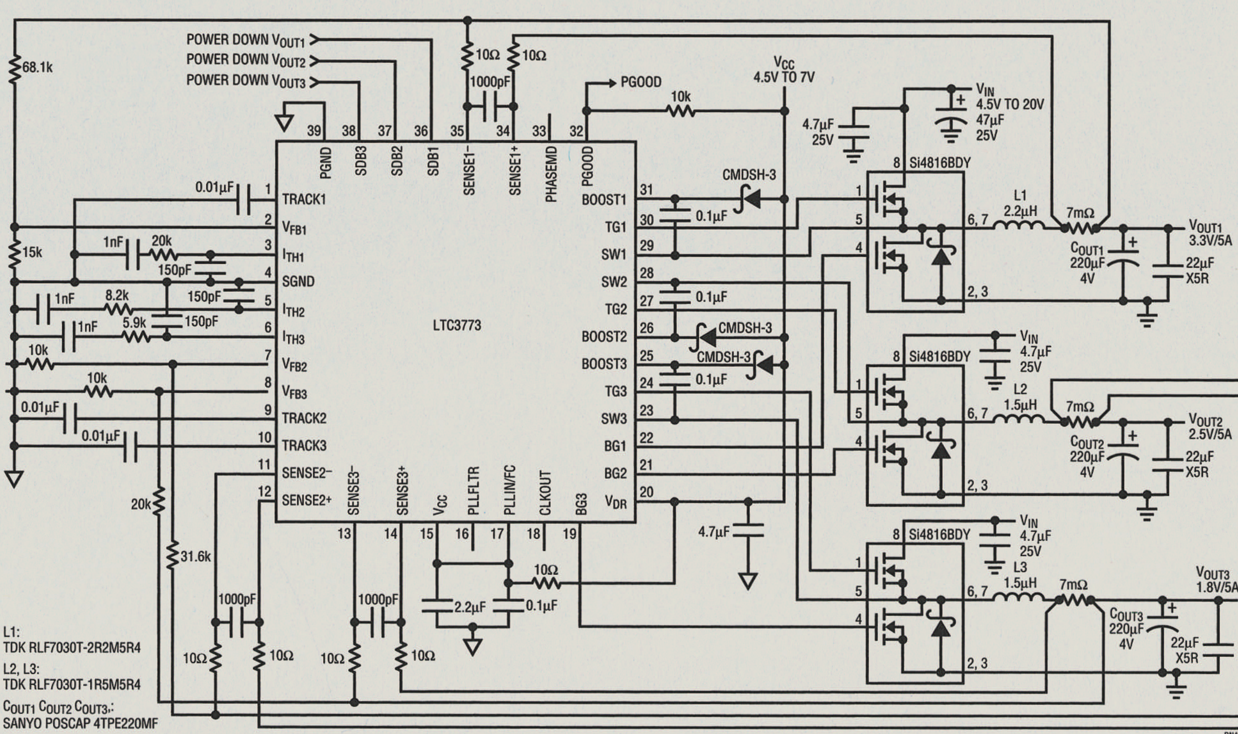

Figure 1. High Density 5A Converter. Total Circuit Size = 1.5in², with Components on Both Sides

Switching the three rails out of phase results in improved performance and reduced cost. The use of triple phase operation instead of single phase can result in a reduction of the input capacitor ripple current by over 50% as shown in Figure 3, allowing the use of less input capacitance. The outputs of two or more phases can be tied together which results in output ripple current reduction as well and a faster load step response. Up to six phases can be synchronized using the CLKOUT pin (on the QFN part only). Fast and accurate current sharing among the parallel phases is a result of the LTC3773's peak current mode architecture.

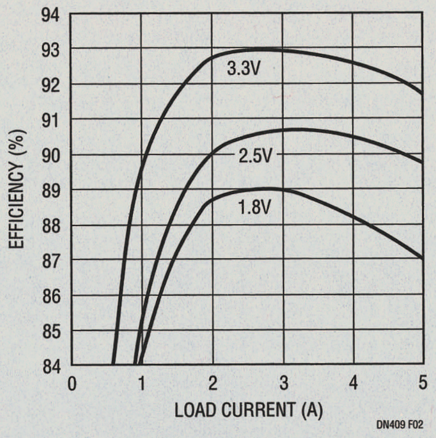

Figure 2. Efficiency of the LTC3773 Converter at V_{IN} = 12V, f_{SW} = 400kHz. One Rail Enabled at a Time

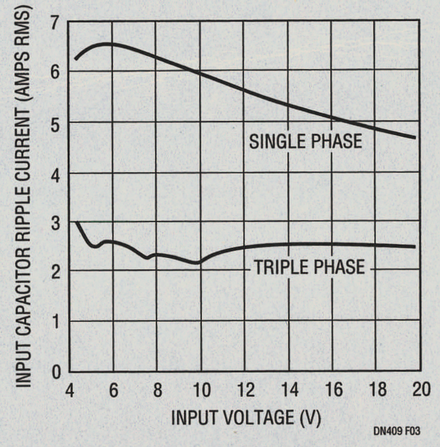

Figure 3. Input Capacitor Ripple Current Comparison for Single Phase and Triple Phase Operation
V_{OUT1} = 3.3V/5A, V_{OUT2} = 2.5V/5A, V_{OUT3} = 1.8V/5A
Single Phase: $\phi_{1,2,3} = 0^\circ$
Triple Phase: $\phi_{1,2,3} = 0^\circ, 120^\circ, 240^\circ$

Compensation of each rail is achieved with an RC network on the I_{TH} pin (error amplifier output). The external I_{TH} compensation and the current mode topology allow the designer to easily stabilize a converter with the minimal amount of output capacitance using a variety of capacitor types including conductive polymer, tantalum and ceramic while still achieving a fast load step response (see Figure 4).

Other features of the LTC3773 include rail tracking and sequencing, a PGOOD signal, and three selectable light load operating modes (continuous conduction mode, Burst Mode® operation and pulse skip mode).

Conclusion

Now designers have a clear and practical solution when they need a compact and cost effective triple supply rail requirement in their telecom, server or network systems.

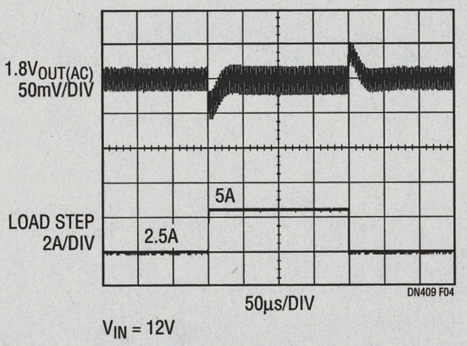

Figure 4. 1.8V Load Step Response

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To obtain a continuously variable duty cycle, **Figure 2** shows how to connect potentiometer R_4 to the common junction of R_1, R_2, and R_3. The output waveform's duty cycle, D_TC, follows the equation: $D_TC=(R_1+R_2+R_{VAR})/(R_1+2R_2+R_3+R_{POT})$, where R_{POT} is the potentiometer's end-to-end resistance, and R_{VAR} is the fraction of R_{POT} between the rotor and R_1. As the equation shows, D_TC depends linearly on R_{VAR}. Switch S_1 comprises one section of a 4066 CMOS quad bilateral SPST switch, IC_2.

You can use the circuit in **Figure 3** to evaluate duty-cycle linearity. A rotary switch and a tapped series string of 16-kΩ resistors provide a 10-kHz signal with nine discrete, equally spaced duty-cycle values ranging from 2 to 98%. For accurate results, use a 5½-digit multimeter to match the values of resistors R_4 through R_{11} and a Tektronix 3012 oscilloscope or equivalent to gather D_TC data.

Microsoft's (www.microsoft.com) Excel-spreadsheet software includes a linearity analysis that returns the following trend line for the duty-cycle measurements: $D_TC=0.7565\times R_{VAR}+2.1548$; $R^2=1$. The value of 1 for R^2 as Excel calculates shows that the transfer function is perfectly linear. Switch S_1's on-resistance and particularly its leakage current slightly affect the D_TC-versus-R_{VAR} equation's slope and intercept, but the equation remains strictly linear. Using only one of IC_2's four switches eliminates leakage effects and crosstalk that would occur if other circuits used the remaining switches. In addition, using moderately low values for the resistor network further reduces leakage-current effects on circuit performance.EDN

Drive a blue LED from a 3V battery

Sergi Sánchez, Federal Signal Vama SA, Vilassar de Dalt, Spain

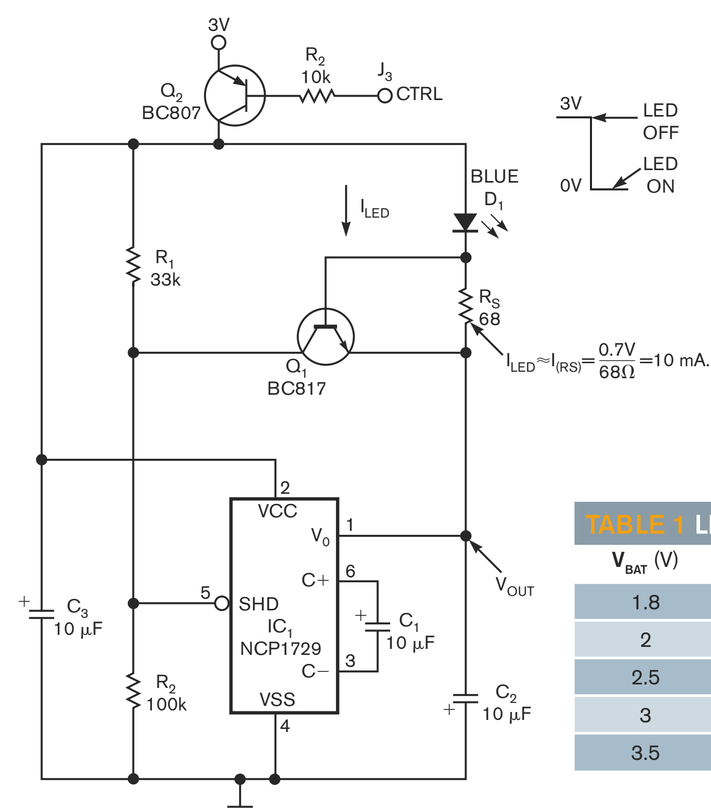

Figure 1 This circuit uses the On Semiconductor NCP1729 voltage inverter, IC_1, to produce enough voltage to drive blue LED D_1.

Using a blue LED can pose problems when available power-supply voltages don't meet or exceed the LED's 3V forward-voltage drop. This Design Idea shows how to drive a blue LED from a 3V battery or another power supply. The circuit in **Figure 1** uses the On Semiconductor (www.onsemi.com) NCP1729 voltage inverter, IC_1, to produce enough voltage to drive blue LED D_1. Transistor Q_1 serves as a constant-current limiter for the LED's forward current. When current through the LED and R_S increases to a level that develops enough base-emitter voltage to turn on Q_1, Q_1's collector draws current from the voltage divider comprising R_1 and R_2 and forces IC_1 to shut down. The voltage inverter restarts when the voltage drop across R_S falls below Q_1's base-emitter turn-on threshold. Pulling transistor Q_2's base to ground through R_2 turns on the circuit.

In this application, the LED exhibits a voltage drop of approximately 3.3V at 10 mA forward-bias current. **Table 1** illustrates the LED's applied voltage, $V_{BAT}+|V_{OUT}|$, and Q_1's base-emitter voltage for various battery-voltage values.EDN

TABLE 1 LED APPLIED VOLTAGE

V_{BAT} (V)	V_{OUT} (V)	$V_{BE(Q1)}$ (V)
1.8	−1.5	0.41
2	−1.37	0.46
2.5	−0.79	0.42
3	−0.27	0.4
3.5	0.23	0.41

Add simple disable function to a panoramic-potentiometer circuit

Lawrence Mayes, Malvern, United Kingdom

In audio-mixing applications, one frequently required function involves mixing a monaural or single-channel source into a stereo-sound field. Audio engineers refer to a panoramic-potentiometer circuit as a circuit that generates left and right signals of correct amplitudes from a monaural signal and places the signal's image anywhere in a stereo-sound field. For the image's loudness to appear independent of its final position, the derived left and right signals must add to produce a constant-power signal rather than a constant-voltage signal.

The widely used circuit in **Figure 1** performs this function by dividing the monaural signal between the two stereo channels and varying each channel's gain between zero and M such that at R_7's centered position, each channel's gain is 0.707M. If you calculate component values to achieve these conditions, then the circuit presents the remarkable property that, for all positions of R_7's wiper, the sum of the powers in the left and right channels is constant to within 0.19 dB.

You can use a DPDT switch, S_1, to bypass the circuit and thus remove it from the audio chain (**Figure 2**). As an alternative, you can add two resistors and use an SPST switch to disable or enable the circuit. The circuit in **Figure 3** presents the same gain characteristics as in **Figure 1**. Closing switch S_1 enables the panoramic-potentiometer function, and opening the switch produces a fixed central-sound image. Additionally, from a practical viewpoint, the circuit of **Figure 3** simplifies wiring and introduces no significant switching transient because enabling the panoramic-potentiometer function involves only grounding R_7's wiper. Even when you use preferred-value components and disregard component tolerances, the circuit introduces a maximum gain error of only 0.21 dB. **EDN**

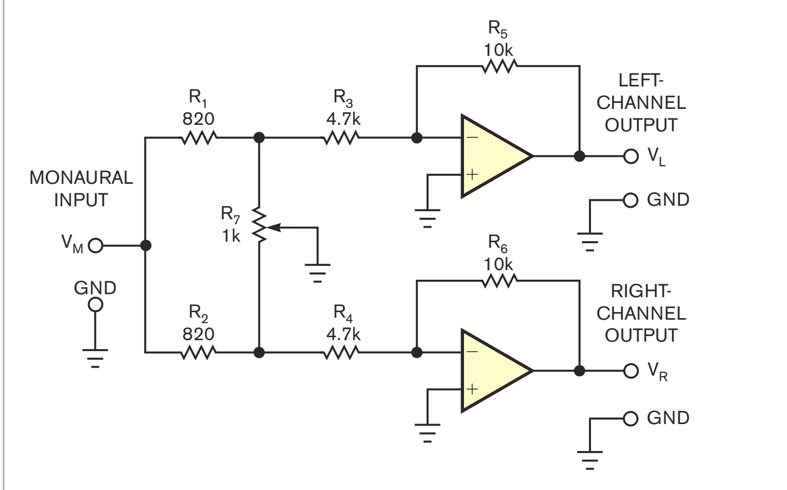

Figure 1 In this basic panoramic-potentiometer circuit, the position of R_7's wiper controls the position of a monaural image in a stereo audio signal.

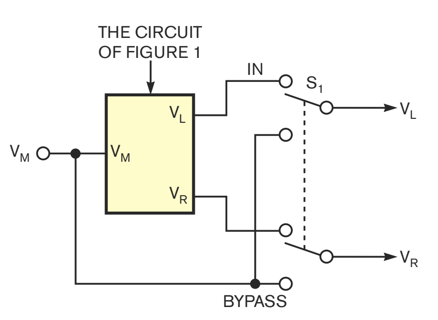

Figure 2 A DPDT switch removes the panoramic potentiometer but introduces wiring complexity and transients.

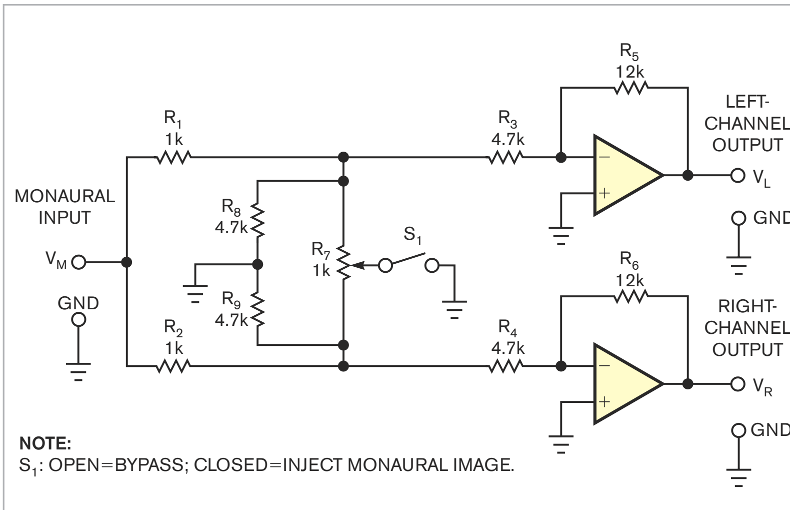

Figure 3 Adding resistors R_7 and R_8 and SPST switch S_1 simplifies wiring and minimizes transients.

Simple single-cell white-LED driver uses improvised transformer

Jim Grant, Scientific Controls, Orlando, FL

A white LED delivers a wide color spectrum and better visibility than do monochromatic LEDs. However, a white LED presents a higher forward-voltage drop than do its colorful counterparts and thus poses problems for operation from a single 1.5V cell. The self-oscillating step-up converter in **Figure 1** features a minimal component count and an easily assembled transformer, T_1.

During the time it takes to charge T_1's primary inductance, resistor R_1 and T_1's added secondary winding provide sufficient base current to turn on Q_2. Q_2's collector current increases until its base current can no longer hold the transistor in saturation. When Q_2 comes out of saturation, T_1's magnetic flux and secondary-voltage polarity reverse. During T_1's primary-discharge interval, the combination of T_1's secondary voltage in series with Q_1's base-emitter voltage applies reverse bias to Q_2's base and turns off the transistor. When Q_2 turns off, the voltage across T_1's primary inductance adds to the battery voltage and applies a forward bias to the LED, D_1. The current through R_1 determines the power applied to the LED and applies forward bias to Q_1's base-emitter junction to provide temperature-compensated bias voltage for Q_2.

The breadboarded circuit's transformer, T_1, comprises eight turns of AWG #30 insulated wire wound around the body of an unshielded 100-μH axial-lead inductor, producing approximately 400 mV p-p across the secondary winding. (**Editor's note:** Observe the winding's polarity dots. If the circuit fails to oscillate, reverse the connections to either the primary or the secondary winding.) The circuit operates over an input voltage range from just above Q_1's base-emitter voltage drop of approximately 0.6V to the LED's forward-voltage drop of approximately 3V. The circuit's switching frequency exceeds 340 kHz at 1.5V input. **EDN**

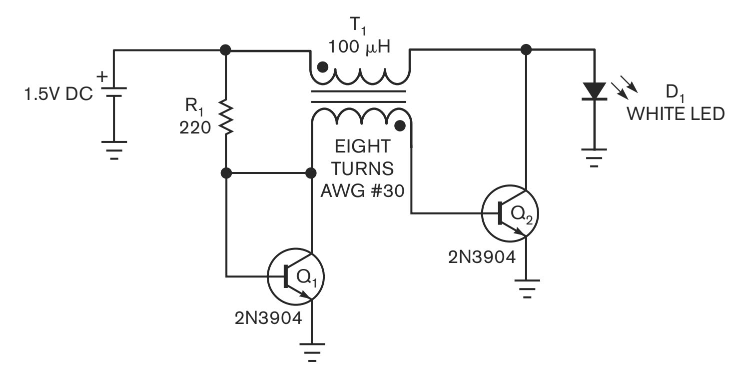

Figure 1 Two transistors and an easily assembled transformer drive a white LED from a single 1.5V battery.

Implement a stepper-motor driver in a CPLD

Stephan Roche, Santa Rosa, CA

Based on the Motorola (now Freescale, www.freescale.com) heavily used but obsolete SAA1042 stepper-motor-driver IC, this Design Idea describes a CPLD (complex-programmable-logic-device)-based implementation of a stepper-motor driver that can also replace the driver in SAA1027- or UCN5804B-based designs. The design uses only six macrocells of a Xilinx (www.xilinx.com) XC9536 CPLD and thus can implement multiple stepper-motor drivers in one small-capacity CPLD. The CPLD stepper-motor driver requires clock, direction, step-size, and reset inputs. The clock input accepts logic-level pulses and goes active on the pulse's positive edge.

The direction, or CW/CCW (clockwise/counterclockwise), input determines the motor's rotational direction. Depending on the motor's electrical connections, holding this input at 0V normally produces CW rotation, and a logic-1 input produces CCW rotation. The step-size—that is, full- or half-step—input determines the motor's angular rotation for each clock pulse. Holding this input low commands the motor to execute a full step for each applied clock pulse, and a high input

TABLE 1 DRIVER OUTPUTS FOR EACH MACHINE STATE

Outputs	Step 0	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7
A	0	0	1	1	1	1	0	0
A_n	1	1	1	0	0	0	0	1
B	0	0	0	0	1	1	1	1
B_n	0	1	1	1	1	0	0	0

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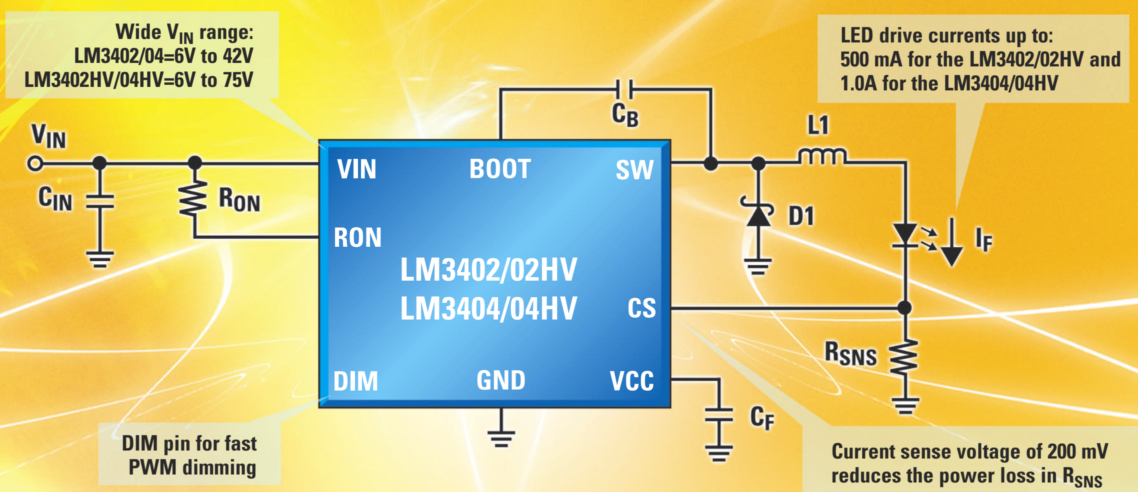

LM3402/04 Features

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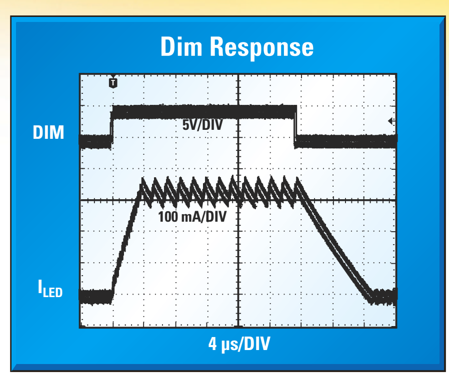
- Constant on-time control with voltage feed-forward for nearly constant switching frequency over the full line voltage range
- Low 0.2V feedback reference minimizes power losses
- Low shutdown current when R_{ON} pin held low
- High voltage capability supports long strings of LEDs
- Choice of 0.5A or 1.0A peak current capability (LM3402/LM3404)



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produces a half-step. A high level on the reset input puts the motor in a previously defined state and commands the CPLD to ignore any incoming clock pulses.

The CPLD's outputs comprise A and A_n and B and B_n phases, each of which controls one of the motor's two coils through external power drivers IC_2 and IC_3, which operate at the motor's nominal voltage (**Figure 1**). A pair of Schottky diodes at each driver's output protects the drivers' outputs during inductive-voltage transients induced by reversing the windings' currents. Using MOSFET drivers with internal diodes, such as Microchip's (www.microchip.com) TC4424A dual driver, may eliminate the requirement for external diodes.

The CPLD's program comprises an eight-state Moore finite-state machine that corresponds to the motor's eight half-step states. **Table 1** shows the driver's outputs for each machine state. In full-step state mode, the state machine executes only Step 0, Step 2, Step 4, and Step 6. At each clock pulse's rising edge, the machine state changes from Step(n) to Step(n+1) if CW/CCW is high or from Step(n) to Step(n−1) if CW/CCW is low. You can download a generic VHDL implementation of the stepper-motor-driver firmware from this Design Idea's online version at www.edn.com/070215di2. Although written for an XC9536 CPLD, the code is also suitable for any CPLD or FPGA target device.**EDN**

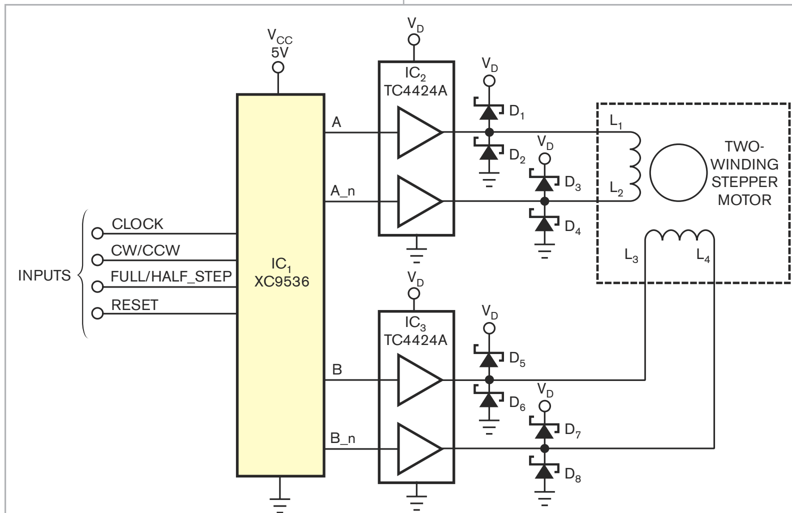

Figure 1 Emulating a dedicated stepper-motor controller, a programmable-logic device, IC_1, applies stepper-motor signals to motor drivers IC_2 and IC_3.

productroundup

SWITCHES AND RELAYS

16A relay comes in subminiature package

Able to switch 16A at 250V ac, the G5LE-E power pc-board relay series comes in 19.6×22.5×15.2-mm packages. Available with coils in 5, 12, and 24V dc, the devices have 360-mW power consumption. The relays have a 4.5-kV impulse-withstand voltage. Prices for the G5LE-E relays range from 75 to 85 cents (5000).

Omron Electronic Components, www.components.omron.com

Current-sensing IPS targets automotive systems

Switching as much as 100A, the IR33x high-side IPS (intelligent-power-switch) family features accurate current sensing and built-in protection circuits suiting 14V automotive applications. In PWM (pulse-width-modulator)-controlled applications, the accurate-current-sensing feature provides feedback, allowing a microcontroller or an ASIC to control the load current. Additional features include a ±5% current feedback at maximum load current and a 100-kHz feedback bandwidth, suiting applications with a low-side switch, providing high-frequency PWM, and providing protection and load-current sensing for unidirectional dc-motor-drive applications. The devices integrate overtemperature and overcurrent shutdown as well as reverse-polarity protection. In the case of a reverse-battery condition, an integrated protection circuit turns on the main MOSFET switch, relieving the intrinsic body diode and reducing thermal problems. The family also provides ESD protection and an active clamp circuit for safer operation and protection in harsh environments. Prices for the IR33x range from $1.44 to $1.95 (10,000).

International Rectifier, www.irf.com

SSR provides voltage insulation in miniature packaging

The ASSR-1410/1420 SSR (solid-state relay) provides 3.75 kV of insulation protection. The 60V, 0.6A, 1Ω devices come in a 1 Form A, single-channel SSR with MOSFET output in an SO-4 package and in a 2 Form A, dual-channel SSR in a DIP-8 package. The ASSR-1410 and -1420 cost $1.48 and $2.49 (10,000) in SO-4 and DIP-8 packages, respectively.

Avago Techologies, www.avagotech.com

Reflective infrared switch provides a 3-in. reflective distance

Providing long-distance sensing that suits machine-automation safety switches, the OPB732 series has a reflective distance over 3 in., depending on circuitry and reflective material. This noncontact infrared switch includes an opaque house, reducing the sensor's ambient-light sensitivity. Features include an 850-nm wavelength, a 100-nW power dissipation, a 50-mA maximum forward current, and a 1.8V maximum forward voltage, as well as a 3V reverse dc voltage with a 100-µA reverse current. Aiming at door closures, end-of-travel indicators, short-distance safety curtains, and product-positioning systems, the OPB732 reflective switch costs $2.97 (1000).

Optek Technology, www.optekinc.com

GaAs RF switches have low insertion losses

Targeting front-end applications, the RF1200 and RF1450 GaAs (gallium-arsenide) pHEMT (pseudomorphic-high-electron-mobility-transistor) RF high-power switches suit multimode GSM/WCDMA cellular handsets, antenna tuners, and cellular infrastructure. Meeting WCDMA requirements, the RF1200 SPDT (single-pole double-throw) switch provides a 0.35-dB insertion loss at 1 GHz, a 25-dB isolation at 1 GHz, 2.6 to 5V control voltage, and

SWITCHES AND RELAYS

−80-dBc harmonics H2 at 1 GHz. The RF1450 SP4T (single-pole four-throw) switch provides a 0.6-dB maximum insertion loss, a 15-dB isolation at 2.2 GHz, 2.6 to 5V control voltage, and −75-dBc harmonics at 1 GHz. Additionally, the switch features increased linearity performance suiting multimode WCDMA applications and integrated decoding logic, allowing two control lines for switch control. Fabricated with a 0.5-μm GaAs pHEMT process, the RF1200 comes in leadless QFN-6 packaging and measures 2×2 mm; the RF1450 comes in a QFN-16 package and measures 3×3×0.6 mm. The RF1200 costs 59 cents (10,000), and the RF1450 costs $1.19 (10,000).

RF Micro Devices, www.rfmd.com

MICROPROCESSORS

Emulator extends previous generation's voltage range

Replacing the E8 model, the E8a emulator provides C-source-level debugging at full speed with microcontrollers in the M16C, H8/Tiny, or H8/Super-low-profile series. The new support tool extends the operating voltage range to 1.8 to 5V and adds a clock oscillator, enabling asynchronous communication in line with a microcontroller's operating frequency. Providing a plug-and-play USB 2.0/1.1-compatible interface, the emulator operates in bus-powered mode using the USB power supply. Supplying 300 mA at 3.3 or 5V to the connected system, the device also features 255 software breakpoints; four hardware breakpoints, including data and address matches; a forced breakpoint; and a branch-origin PC trace of the last four instructions before a break. In addition, the emulator allows referencing and modification of memory, on-chip I/O, and memory contents while executing a program. The E8a emulator costs $125.

Renesas Technology America, www.renesas.com

Development kit targets eight-pin microcontrollers

Based on the ST7-FLITEUS microcontroller, the ST7FUS-Primer USB-powered evaluation and development package aims at the vendor's eight-pin ST7Lite microcontroller family. The vendor's UltraMusic application highlights the internal RC oscillator, the 10-bit ADC, the 12-bit autoreload timer with PWM (pulse-width modulation), and the low- and auxiliary-voltage detectors. Additional features include a C compiler, a RIDE software tool set, the RBuider application builder, the RFlasher programming interface, and the Raisonance uRLink in-circuit debugger. The in-circuit debugger allows users to run, modify, and debug application code on the host computer through a USB connection. Measuring 4.5×3.5 mm in a DFN-8 package, the ST7FUS-Primer costs $12.

STMicroelectronics, www.st.com

DSP controllers have a high-resolution PWM

Providing a 32-bit-wide datapath, the four 60-MHz TMS320F280xx DSP-based controllers include an on-chip, 12-bit ADC and QEP (quadrature-encoder-pulse) interfaces. A timer captures and compares the signal output with 10 independent PWM (pulse-width-modulation) channels. Communications interfaces include CAN (controller-area-network), I²C, UART, and SPI ports, depending on the device. The controllers use a 150-psec resolution PWM, providing 16-bit accuracy in a 100-kHz control loop and 12-bit accuracy at 1.5 MHz. Available in an LQFP-100 package, the devices are AEC Q100-automotive-qualified. The TMS320F280xx costs $3.25. The TMS320F2808 eZdsp development kit allows developers to program the controllers; the kit costs $495.

Texas Instruments, www.ti.com

EDN

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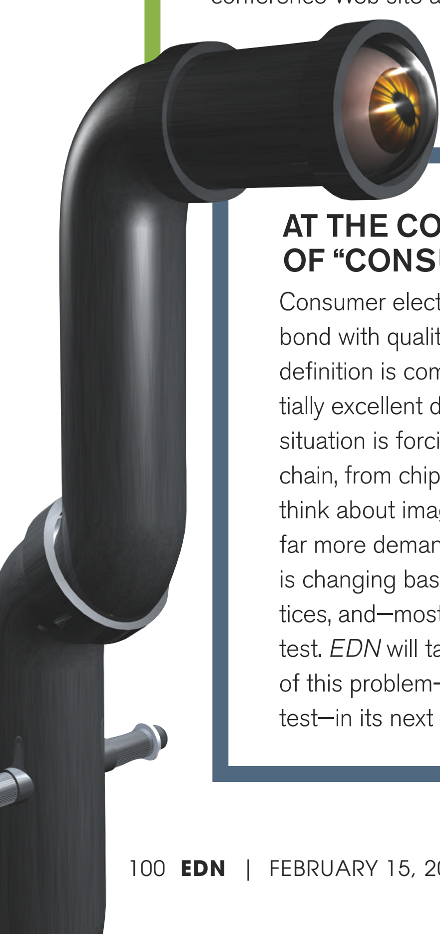
LOOKING AHEAD

TO ISQED, SPEAKING OF QUALITY

The eighth International Symposium on Quality Electronic Design takes place March 26 through 28 at the DoubleTree Hotel in San Jose, CA. This quiet conference has established itself as one of the few venues in which participants discuss the final quality of IC-based systems in a multidisciplinary environment. Key topics this year will include the apparent conflict between product quality and time-to-market demands; the process of quickly bringing an IC-based product to volume production; and the roles of platform-based design, methodology adjustments, and embedded quality-assurance structures in taking on the growing challenge of electronics quality. Visit the conference Web site at www.isqed.org.



LOOKING AROUND

AT THE CONCEPT OF "CONSUMER QUALITY"

Consumer electronics has not had a strong bond with quality over the years. But high definition is coming to video, bringing potentially excellent digital audio along with it. This situation is forcing everyone in the supply chain, from chip vendors on up, to at least think about image and sound quality in new, far more demanding ways. And that thinking is changing basic assumptions, design practices, and—most painfully—manufacturing test. *EDN* will take a hard look at one aspect of this problem—audio characterization and test—in its next issue.

LOOKING BACK

AT THE BEGINNINGS OF FAULT-TOLERANT COMPUTING

A 26-month reliability program conducted on an experimental digital differential analyzer computer produced only 25 instances of erratic operation of components. Incorporating built-in test equipment, this computer's circuitry, which is designed to operate all units at the lowest functional input rate, is said to assure a high degree of accuracy. During the computer's development, a program of thorough testing of available tubes, resistors, diodes, and other components commenced, defining three types of tolerance for every unit. These were termed purchase tolerance, removal tolerance, and failure tolerance. "Purchase tolerance" is described as a perfect new part, "failure tolerance" is that of a part showing minimum remaining operative capability, and "removal tolerance" is a component operating midway between the two—the point at which it should be replaced during routine maintenance. The computer's circuitry was then designed to operate with all components at failure tolerance, ensuring that components are removed well before an actual failure occurs.

—*Electrical Design News*, February 1957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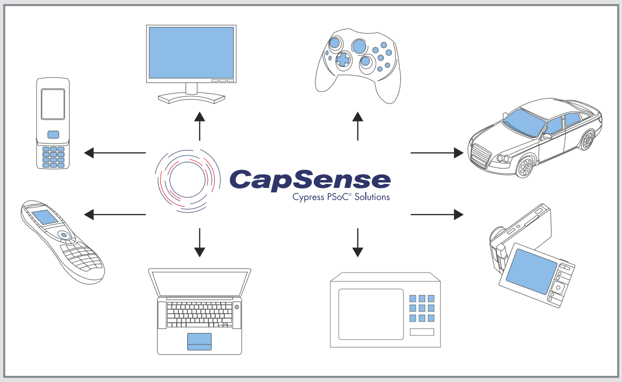

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